1989

The development of LSI grade logic families for digital GaAs integrated circuits /

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THE DEVELOPEMENT OF LSI GRADE LOGIC FAMILIES FOR DIGITAL GaAs INTEGRATED CIRCUITS

by

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A Thesis

Presented to the Graduate Commitee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University

1989

Certificate of Approval

This thesis is accepted and approved in partial fullfillment of the requirements for the degree of Masters of Science in Electrical Engineering.

May 18, 1989
(date)

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ACKNOWLEDGEMENTS

I would like to thank my advisor Professor Frank Hielscher for his time and helpful comments. I would like to thank Donna Robertson and Perry Robertson for their typing and editorial comments. I would like to thank the Management at Bell Laboratories, Reading, PA for their support and for allotting time to me to work on my Master's program.

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ABSTRACT

Three logic families have been developed which are capable of realizing low power and high speed LSI/VLSI digital GaAs integrated circuits. The logic families are Source Follower Logic (SFL), Push/Pull SFL, and FET Injection Logic (FIL). These families are analyzed and compared to the traditional Direct Coupled FET Logic (DCFL) family.

Three input NOR/NAND gate 7 stage ring oscillators were laid out in AT&T's SARGIC process, which uses MBE grown Hetro-junction FETs (HFETs) having 1 μm gates. This process utilizes a 2 μm pitch double level metal interconnect technology. The circuits were simulated using AT&T's ADVICE circuit simulator using the nominal, high current and low current model parameters.

The simulation results show that the SFL, Push/Pull SFL and FIL Logic families have higher DC and AC noise margins than DCFL. However, DCFL has the lowest propagation delay and power dissipation due to its small voltage swing (0.5 V). DCFL also generally implements circuits with a smaller FET count which results in smaller chip area.

CHAPTER 1

INTRODUCTION

GaAs integrated circuits are increasingly finding applications in solving system critical path delays. The low power and high speed characteristics of digital GaAs ICs' are a major improvement for high performance digital systems that are silicon based and rely on ECL logic. However, GaAs has not demonstrated a technology capable of achieving LSI and VLSI integration densities demanded by system designers. Most problems stem from the poor process control in present GaAs technology, and the low noise margins of certain logic families used. Also GaAs digital circuits are advocated for use in military systems where junction temperature can be as high as 175° C. At such a temperature high noise margin and low power logic families are demanded, which precludes the use of a low power/small noise margins Direct Coupled FET Logic (DCFL). The development of three logic families capable of implementing digital GaAs integrated circuits with low power, high speed, and high noise margins is presented in this thesis.

The application of GaAs technology in high speed digital integrated circuits can be traced to the early development of submicrometer gate length devices for microwave amplifiers. Microwave amplifiers demanded the development and manufacture of 1 to 0.5 μm gate length GaAs FETs. These devices exhibited higher cut-off frequencies, f_t, than any silicon

device. GaAs devices owe their high performance characteristics to the high electron mobility at low electric fields, and to the semi-insulating properties of the material. Early GaAs processes used a mesa isolation technique [1] which resulted in a non-planar topology, and only permitted the realization of Depletion MESFETs' and Schottky barrier diodes, and was limited to one level of interconnect. At present digital oriented processes are planar, realize Depletion (DFET), Enhancement (EFET), and Schottky diodes. These devices are interconnected by a double level metal technology which results in much higher circuit densities than in the past.

The high speed and low power characteristics demanded by next generation computers, signal processing circuits, and instrumentation systems can be easily met by digital GaAs technology. Digital GaAs integrated circuits have demonstrated logic gate propagation delay below 20 pS at a power dissipation below 100 μW. Military systems demand integrated circuit technologies that tolerate a wide temperature range (-55 to 125° C) and greater than $1x10^7$ rads radiation environment. At present these requirements can only be met by GaAs technologies.

Chapter 2 presents some background information about GaAs technology, design trade-offs, and AC/DC noise margin analysis.

Chapter 3 presents a basic formulation of the physics of Hetro-junction FETs (HFETs). The chapter begins by quantifying the two dimensional electron gas (2 DEG) and presenting the current versus voltage and capacitance versus voltage characteristics of HFET devices. The salient characteristics for the HFET devices used in simulating the ring oscillators are given in the last section of Chapter 3.

In Chapter 4, a back-of-the-envelope analysis is performed on the logic families to derive the equations used to calculate the output voltages of the high and low logic states. Also, the unity gain points are derived for the transfer characteristics, and the simulated and calculated transfer characteristics are compared for the logic families under consideration. Finally, chapter 4 shows how complex gates, set/reset and clocked latches can be implemented.

Chapter 5 presents the simulation results for each logic family. This analysis were performed using nominal, high and low current model parameters at 25 and 125° C. Data is presented for propagation delay, power dissipation, fanin/fanout sensitivity, and the power versus delay curves for each logic family.

CHAPTER 2

BACKGROUND

2.1. GaAs Devices

A number of devices can be realized in GaAs technology. The most mature devices are the DFET and Schottky diode structures shown in Figure 2.1. DFETs at present have the highest current drive capability per unit width. The Threshold voltage can be tailored by an ion implant under the gate, similar to MOS technology. By increasing the DFET threshold voltage toward the positive side an Enhancement FET (EFET) is realized. The gate to source drive for an EFET is limited to the turn on voltage of the Schottky diode (0.6 V), which results in poor current drive capability. An EFET is schematically shown in Figure 2.2 (a).

The EFET Schottky gate diode greatly reduces the noise margins of logic gates and circuits that utilize EFETs by limiting the voltage swing. By performing a P implant under the gate of a FET, one realizes a GaAs JFET, Figure 2.2 (b). The JFET extends the gate to source drive for an EFET to 1.2 V, which implements EFET based logic gates with higher noise margins and lower power over the DFET and EFET approach.

2.2. Advantages and Disadvantages of Digital GaAs

GaAs integrated circuits' main advantages over bulk silicon technology are primarily due to the higher electron mobility of GaAs as shown in Figure 2.3, and the use of a semi-insulating substrate. The high electron mobility in GaAs, which is five to six times higher than silicon, leads to velocity saturation of GaAs FETs at a low drain to source voltage. Velocity saturation in GaAs is achieved at about 5000 V/cm, which leads to 0.5v saturation voltage for a 1 μm gate FET. Velocity saturation in silicon is about 20,000 V/cm, which leads to a saturation voltage of 2 V for a 1 μm gate length FET. However, silicon devices saturate below 2 V drain to source voltage due to channel pinch-off.

The lower saturation voltages of GaAs devices exhibit higher average charging and discharging currents over silicon as can be inferred from the drain characteristics of a GaAs FET and a MOSFET in Figure 2.4. Higher charging and discharging currents translate directly to higher gate switching speeds of GaAs integrated circuits. The lower saturation voltages in GaAs also allow a reduction of power supply voltage and voltage swings, hence GaAs circuits have low power delay products compared to silicon circuits as shown in Figure 2.5 [2].

GaAs devices are formed in a floating semi-insulating substrate, which leads to device isolation with much lower capacitance than silicon p-n junction isolation. The

floating substrate results in an interconnect technology with very low substrate capacitance, although GaAs has a higher relative permittivity than silicon, hence circuit delays will be dominated by line to line capacitance. Substrate capacitance in silicon circuits is one of the dominant factors leading to performance degradation.

GaAs technology has a number of device and circuit related disadvantages over silicon. The most severe problem is the lack of a native oxide which prevents the development of a MOSFET structure. Hence, the MESFET is the most widely used structure in mature GaAs technologies. The MESFET suffers from the presence of a parasitic Schottky gate diode that forward biases at 0.6 V, which limits the voltage swing of the Enhancement/Depletion (DCFL) inverter shown in Figure 2.6.

The small voltage swing limits the DC high and low noise margin of DCFL to less than 200 mV at room temperature. This noise margin is not enough to manufacture high yield and high density integrated circuits. Hence, complex and novel logic gates suitable for GaAs have been proposed and investigated as will be shown later. The complicated logic forms employed in GaAs technology consume a large chip area per gate compared to silicon. The increase in area leads to inefficient layouts that degrade circuit performance, reduce circuit yields, and increase cost.

Another serious limitation borne by the MESFET is the inability to use Enhancement mode transmission gates for implementing simple static logic with a single power supply as in MOS silicon technology. This limitation also greatly hampers the development of silicon like high density dynamic circuits and memories. Another less serious shortcoming of GaAs is the lack of P-channel devices, which otherwise could have lead to another degree of freedom in designing low power/high performance GaAs ICs'. The lack of P channel devices can compromise circuit performance, since every GaAs logic family is a ratioed form of logic. This is the same compromising issues of channel width to length ratio (W/L) sizing in NMOS technology. Ratioed logic forms utilize different W/L's for the transistors and have a high ratio of DC to AC power, hence they can be very inefficient when driving high fanout capacitance compared to CMOS technology.

2.3. Design Trade-offs in Digital GaAs Technology

Figure 2.7 shows a simple DCFL inverter driving load capacitances composed of wire Cw and fanout capacitance Cfo. It is assumed the driven loads do not draw any DC current, hence all currents are used to charge and discharge the load capacitance. The average propagation delay from the low to high state t_{pLH} can be calculated as follows:

$$I_C = I_L/2 \qquad (2.0)$$

$$= C_L V_o / t_{pLH} \qquad (2.1)$$

$$C_L = C_w + C_{FO} \qquad (2.2)$$

$$t_{pLH} = 2\, C_L\, V_o / I_L \qquad (2.3)$$

where I_C is the charging current, I_L is the load FET current, V_O is the voltage swing, C_L is the load capacitance which is the sum of wire and input capacitance of the driven stages.

The power dissipation P_D and power delay product are:

$$P_D = I_L\, V_{DD}/2 \qquad (2.4)$$

$$P_D\, t_{pLH} = C_L\, V_o\, VDD \qquad (2.5)$$

The power delay product is directly proportional to the load capacitance CL, voltage swing VO, and power supply voltage VDD. Thus GaAs technology is best operated at low power supply voltages to reduce power dissipation and power delay product. High performance also mandates that the voltage swing be kept as small as possible, as well as reducing the load capacitance. However, reduction of voltage swing directly reduces the circuit noise margins.

Since the ideal sum of high and low noise margins equals the voltage swing VO, reduction of voltage swing can greatly reduce circuit yields and limit integration densities. GaAs technology has demonstrated on-wafer threshold voltage variations as low as 20 mV [1]. However, the small noise margins of most GaAs logic families may not be enough to compensate for such process variation, temperature effects, and system noise to guarantee functionality under all conditions.

The average propagation delay from the high to low state can also be analyzed as shown in Figure 2.8. The average discharge current is given as:

$$I_{DISCH.} = (I_D - I_L)/2 \qquad (2.6)$$

$$t_{pHL} = C_L\, Vo/I_{DISCH.} \qquad (2.7)$$

$$= 2\, C_L\, Vo/(I_D - I_L)$$

where I_{DISCH} is the discharge current and I_D is the driver FET current.

The average propagation delay tp is:

$$t_p = C_L V_o \left[\frac{1}{I_L} + \frac{1}{I_D - I_L} \right] \qquad (2.8)$$

During the high to low transition, the driver FET must discharge the load capacitance, as well as sink the load FET current. This situation is far less efficient than found in silicon MOS technology, since the transconductance and drive capability of silicon MOS devices is much higher.

Most GaAs digital circuits are realized with ratioed logic whereby the noise margins and circuit delay are a strong function of the pull down to pull up device width ratio. Ratioed logic configurations have a high ratio of DC to AC power. Hence, to reduce the propagation delay requires increasing the AC power which is accompanied by a great increase in DC power and a reduction of noise margins.

The power delay product of digital GaAs circuits can be very low compared to silicon technology due to a lower power supply voltage, voltage swing, and lower parasitic substrate

capacitance. However, smaller voltage swings are accompanied by small noise margins which burdens the process to achieve very low process variations. This can be a severe limitation on circuit yields and density, where high yield and high density circuits are essential in a competitive digital market.

2.4. AC and DC Noise Margin Definitions

2.4.1. DC Noise Margins

A digital logic gate's output restores a logic level when the input logic levels are represented by a valid range of voltages. The logic levels of gates generally degrade as they propagate through a digital network, and tend to deviate to outside the allowed range. Hence, the high and low noise margins must be positive under worst case process and temperature variations. Noise margin limits by definition presume the circuit signals to be contaminated with noise to the maximum limit, but yet maintain circuit functionality.

Figure 2.9 illustrates a typical inverter DC transfer curve. The shaded region represents the valid restoring characteristics of the inverter. The logic output value is undefined when the input is between VIL and VIH, where the inverter gain is high [3]. For positive logic, the noise margin high (NMH) and noise margin low (NML) can be expressed

as a function of the valid high (VIH) and low (VIL) input levels and output voltages high (VOH) and low (VOL) as shown:

$$NMH > |V_{OH} - V_{IH}| \qquad (2.9)$$

$$NML > |V_{OL} - V_{IL}| \qquad (2.10)$$

The DC transfer characteristic between the input and output for a gate can be defined for an inverter as:

$$VO = f(VI) \qquad (2.11)$$

Using equations (2.9) and (2.10) [3]:

$$H(f(VOH - NMH) + NML) > VOH \qquad (2.12)$$

$$H(f(VOL - NML) - NMH) < VOL \qquad (2.13)$$

The four logic levels VIH, VIL, VOH, and VOL can be assigned to maximize the noise margin sum for a long chain of inverters. Since a transition at the input of a stage produces an opposite transition at the input of the following stage, maximum circuit noise is maximized by maximizing the high and low noise margin sum. This sum is given as:

$$NMH + NML = H(VIL) - H(VIH) + VIL - VIH \qquad (2.14)$$

By finding the unity gain points of the DC transfer function, one can solve and define the optimum VIL and VIH values as follows.:

$$dH(VIL)/dVIL = -1 \qquad (2.15)$$

$$dH(VIH)/dVIH = -1 \qquad (2.16)$$

This is the definition that will be used in this paper to characterize the DC noise margins.

2.4.2. AC Noise Margins

AC noise margins for a digital gate are applicable under the switching conditions or transient operation. The AC noise margins of a digital circuit are typically smaller than at DC. Figure 2.10 illustrates the transient response of a gate for the ideal and actual cases. A logic gate will experience a loss of noise margin high (ΔNMH) and low (ΔNML). Noise margin loss can be attributed to first order on the following circuit parameters:

A. Voltage swing, VO;
B. Frequency of operation, f;
C. Load capacitance, C_L;
D. Gate propagation delay, t_p.

The AC noise margin (NMAC) can be related to the DC noise margin (NMDC) and loss of noise margin (ΔNM) by the following expression:

$$NMAC = NMDC - \Delta NM \qquad (2.17)$$

$$\Delta NM = VO\ B(f, C_L, t_p) \qquad (2.18)$$

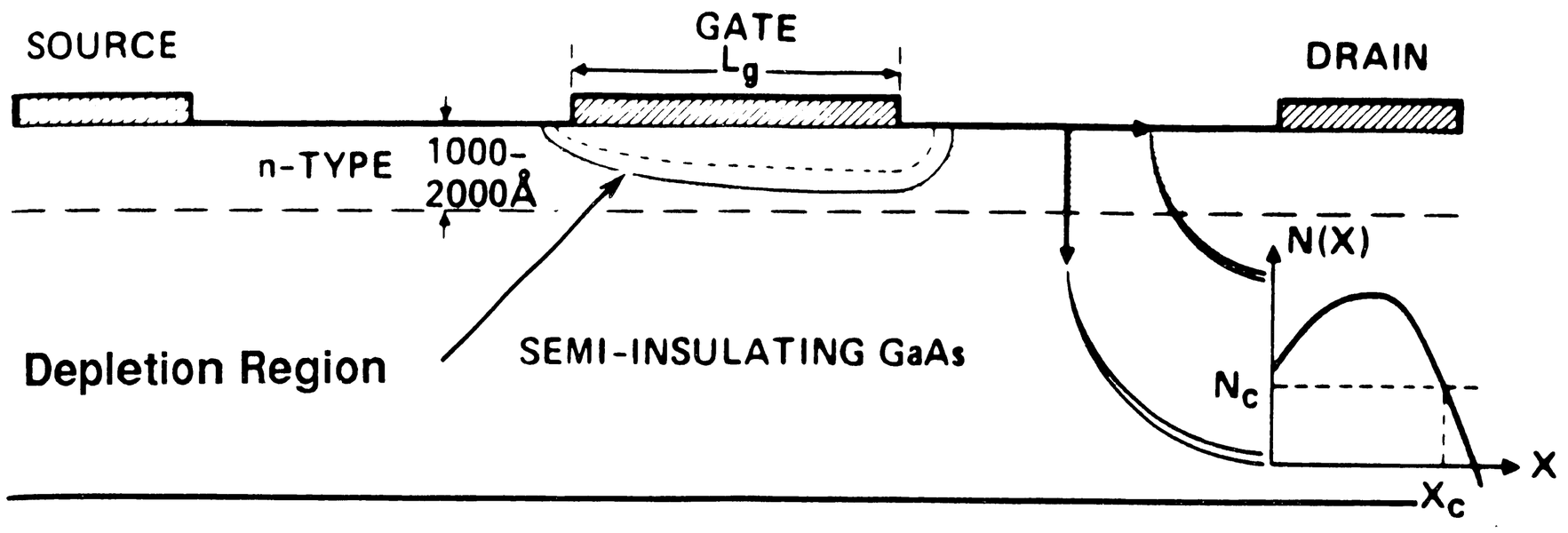
The AC noise margins will be measured by the set-up depicted in Figure 2.11. AC noise margin high is measured by lowering VDD2 and VSS2 simultaneously relative to VDD1 and VSS1 until the circuit fails. The AC noise margin low is measured similarly by raising VDD2 and VSS2 simultaneously

relative to VDD1 and VSS1 until circuit failure. The ACNMH and ACNML can be expressed as:

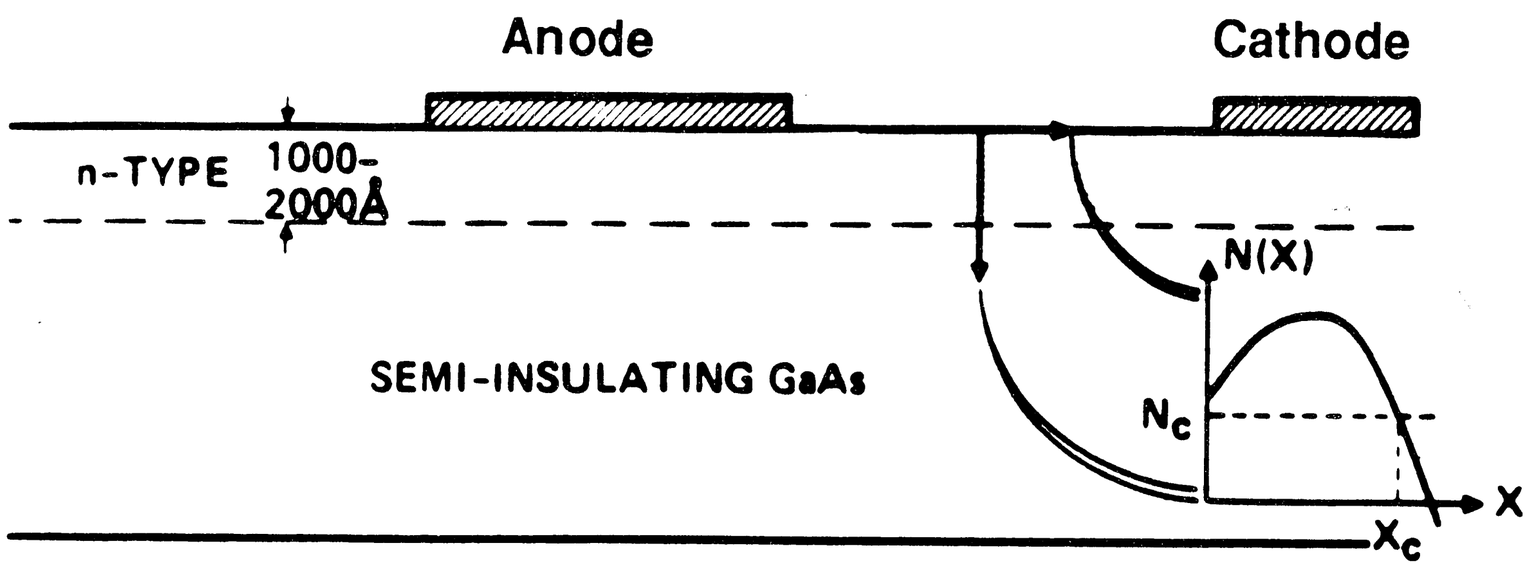
$$ACNMH = |VDD2 - VDD1| \qquad (2.19)$$

$$ACNML = |VSS2 - VSS1| \qquad (2.20)$$

Using this methodology, the AC noise margins for a digital circuit can be measured versus frequency by sweeping the pulse input of a chain of gates.

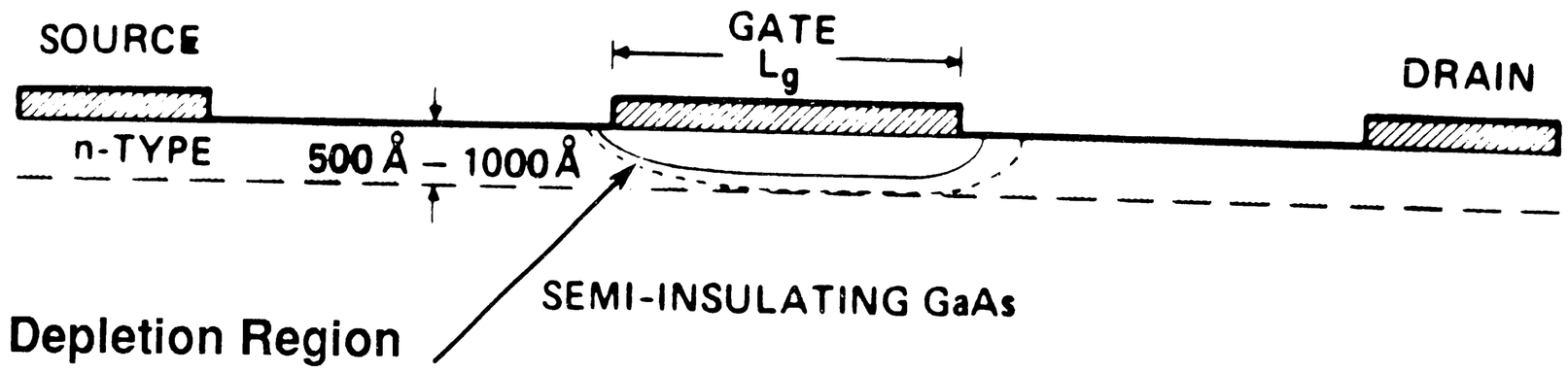


(a)

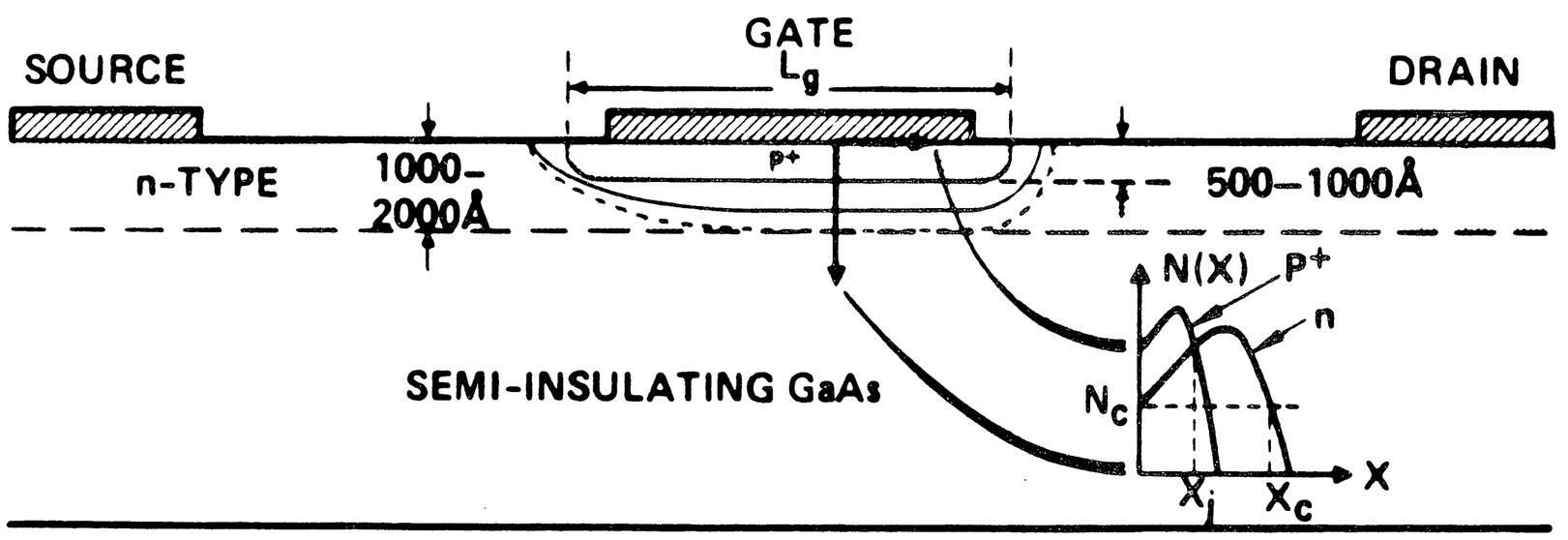


(b)

Figure 2.1. (a) Depletion MESFET, (b) Schottky diode (from ref. [1]).



(a)



(b)

Figure 2.2. (a) Enhancement MESFET, (b) GaAs JFET (from ref. [1]).

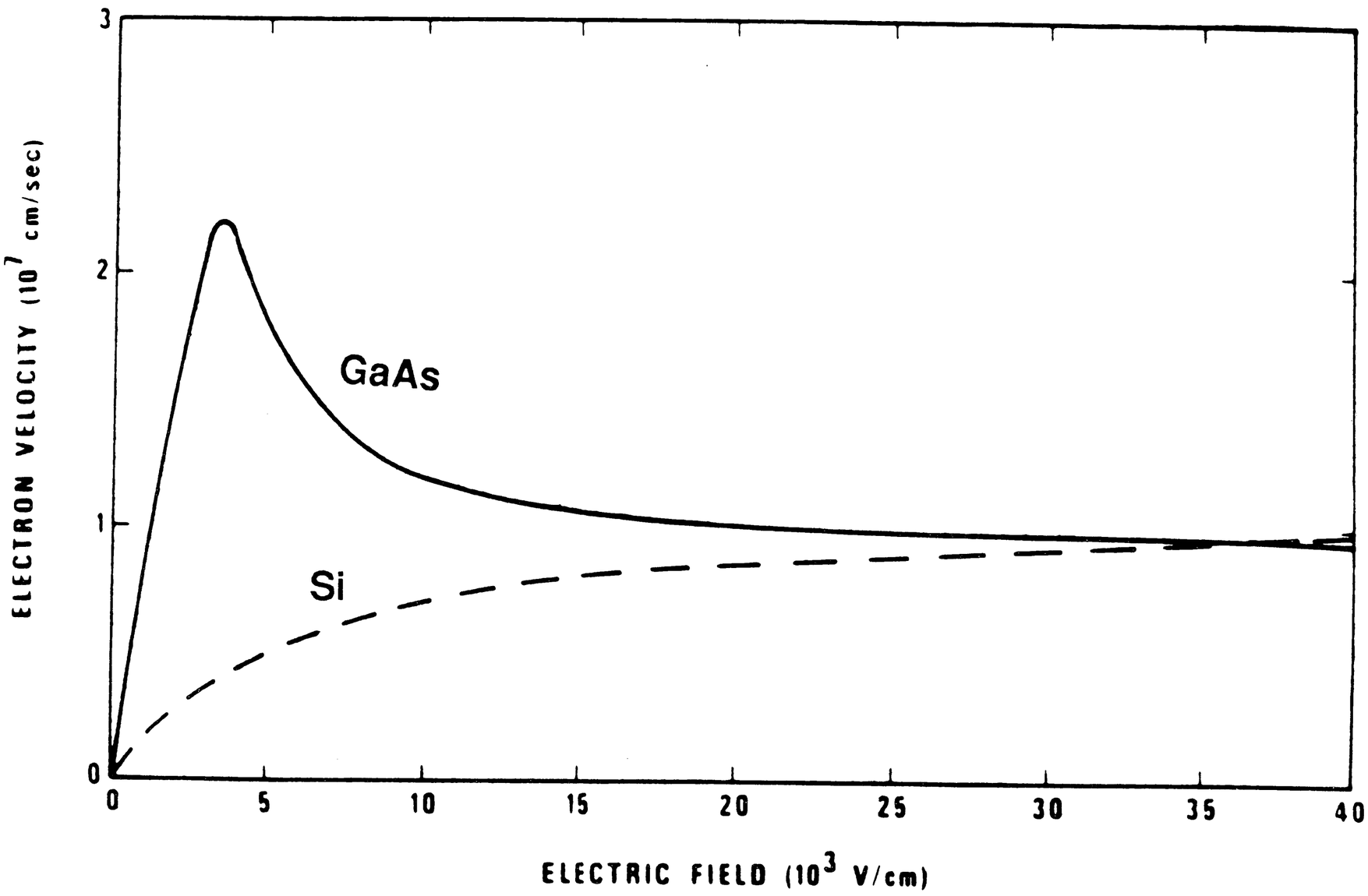
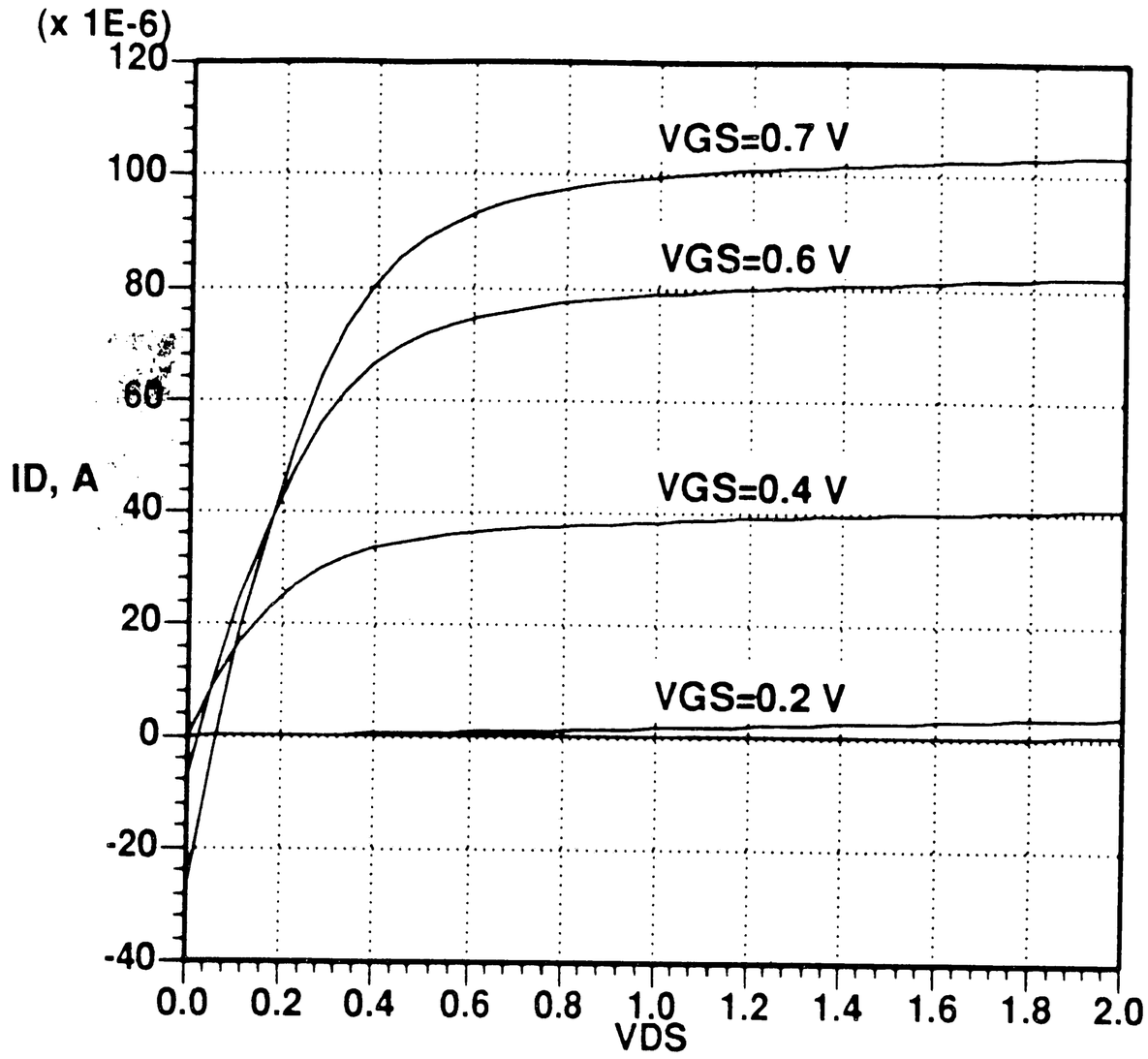


Figure 2.3. GaAs and Si Field Dependant Mobility (from ref. [1]).



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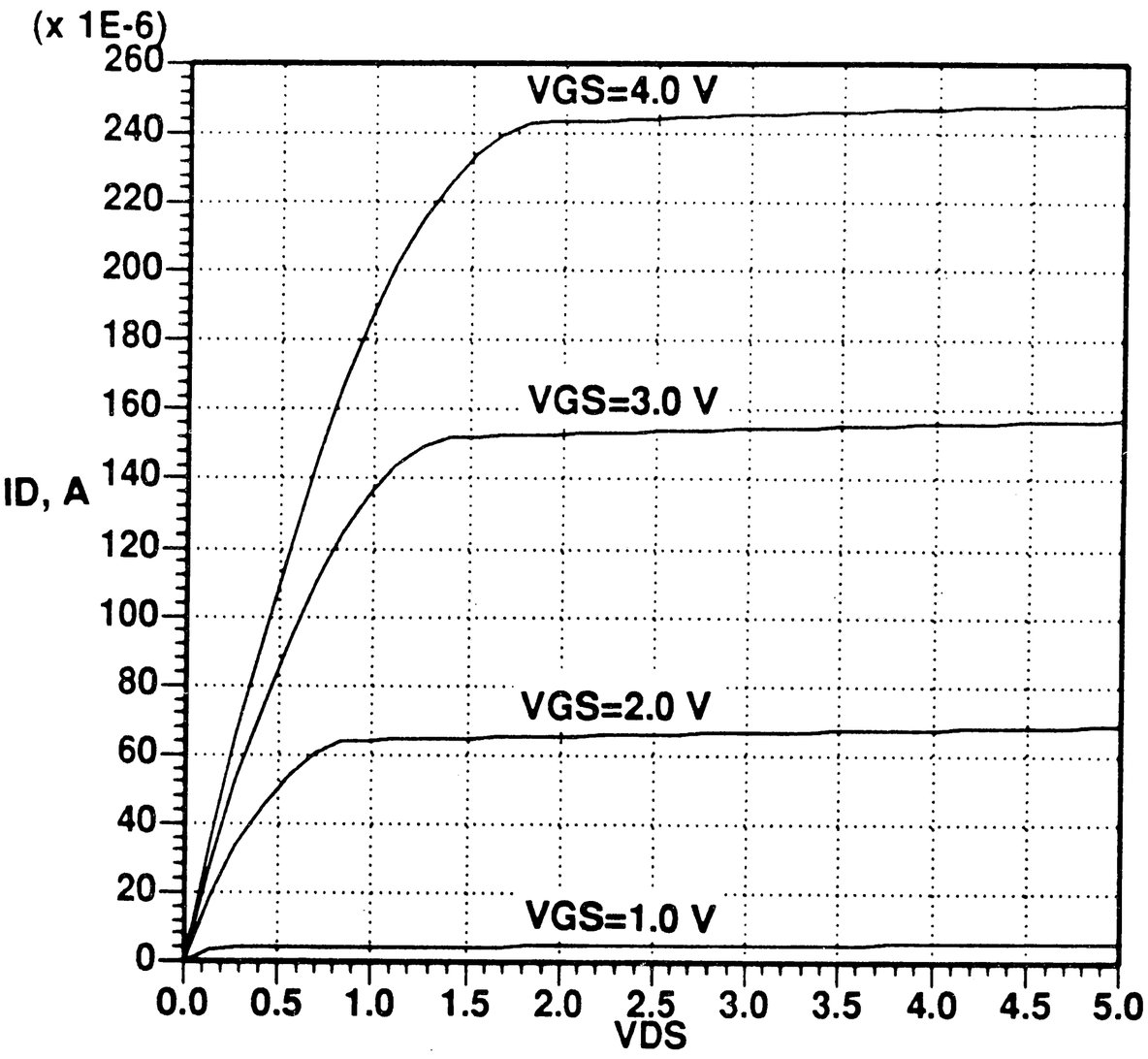


(b)

Figure 2.4. (a) GaAs FET (b) Si MOSFET. Note the different scales for the two devices.

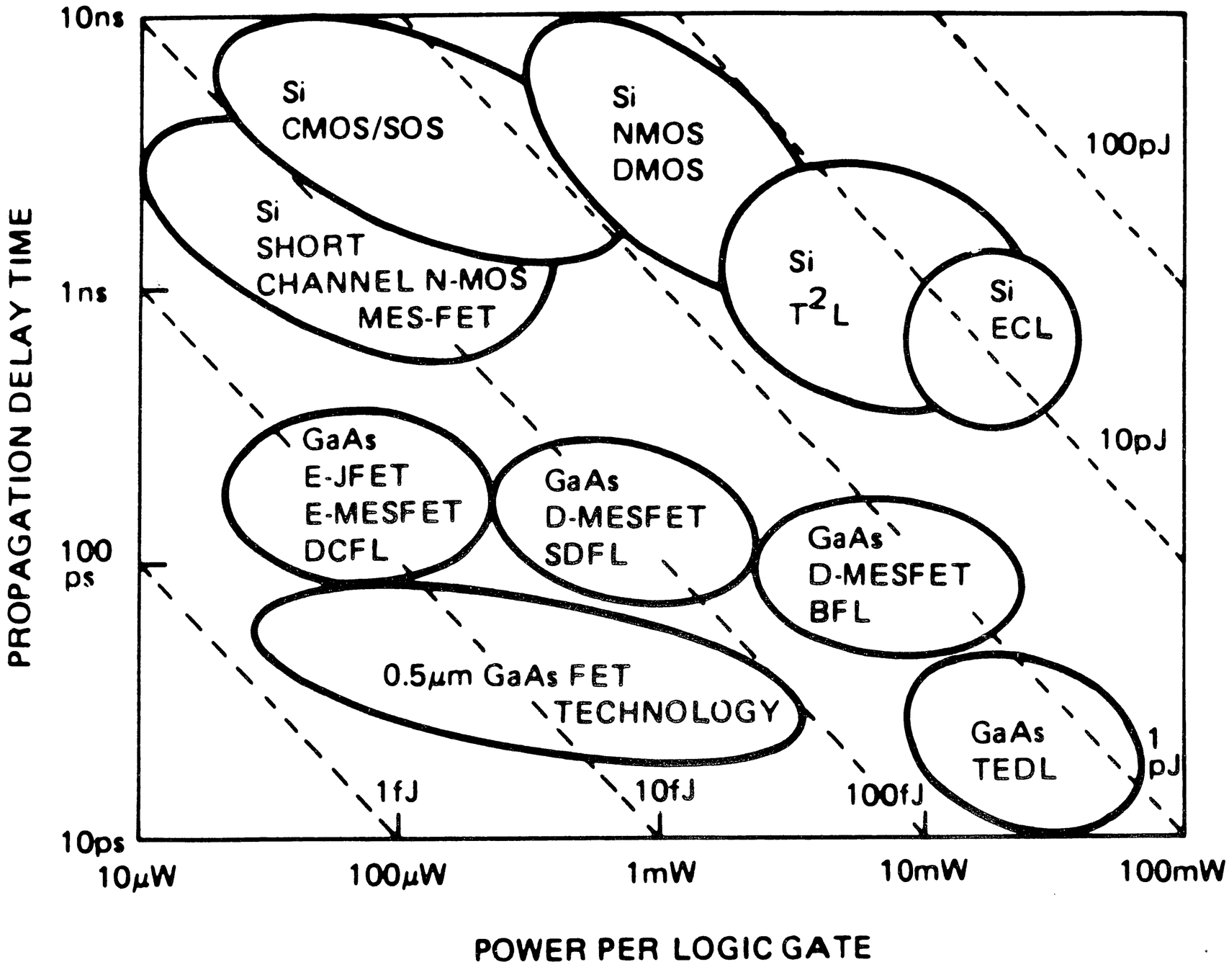


Figure 2.5. Power Delay Product for GaAs and Si Circuits (from ref. [2]).

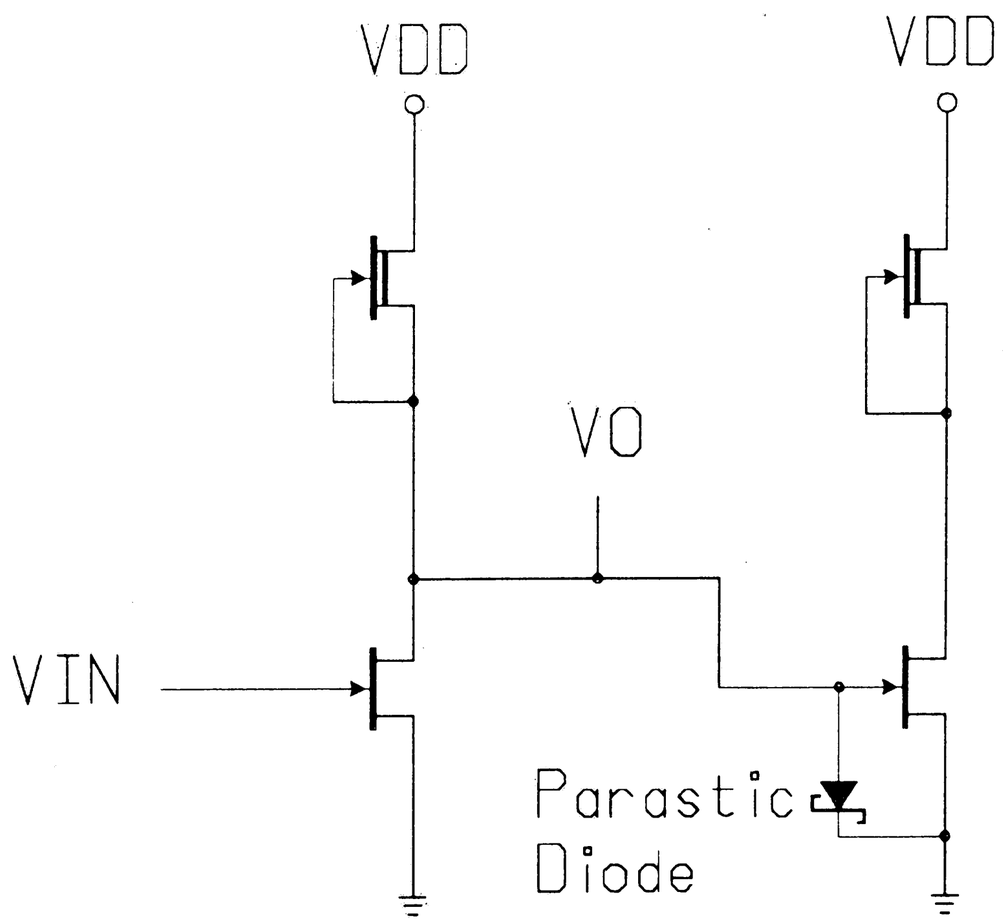
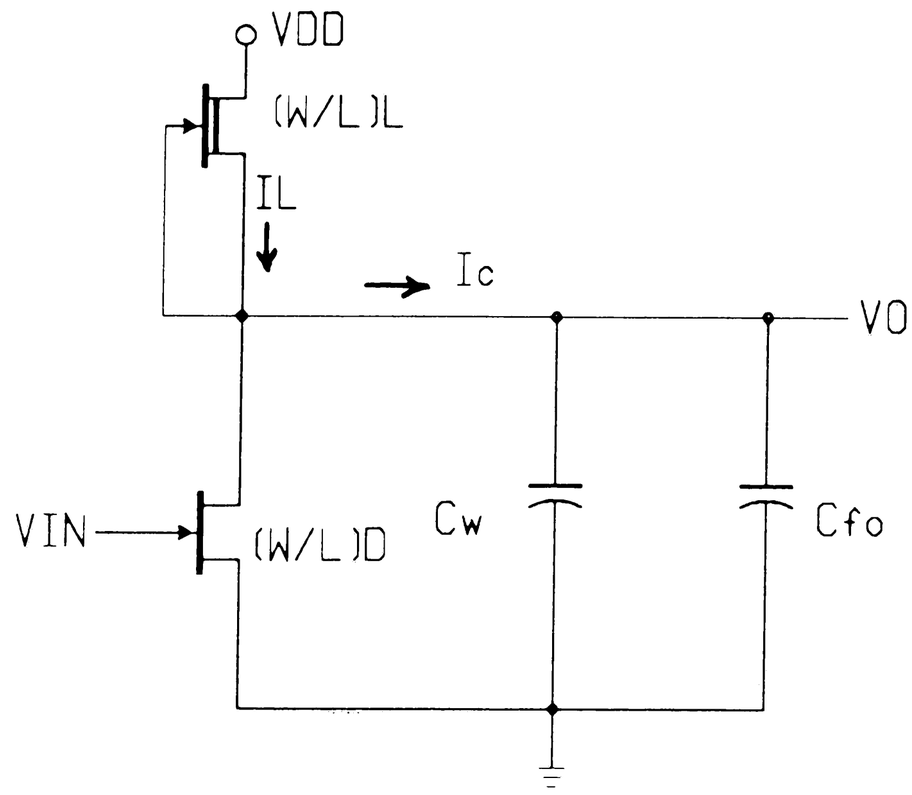
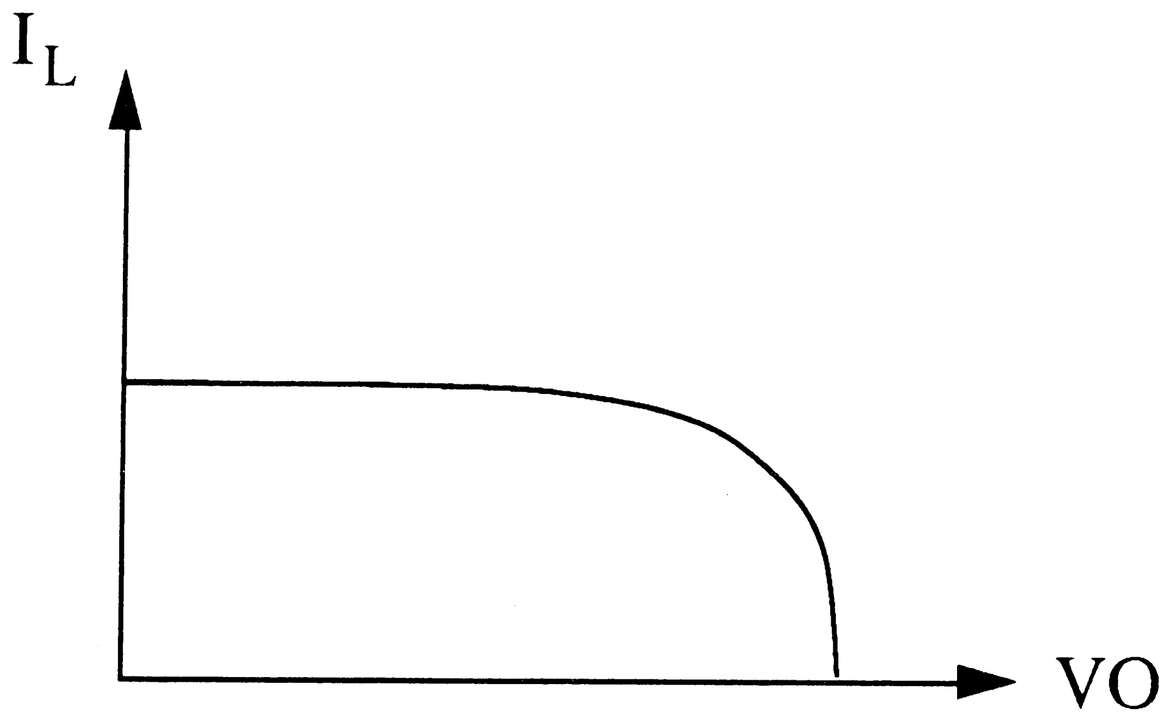


Figure 2.6. Direct Coupled FET Logic (DCFL) Inverter.

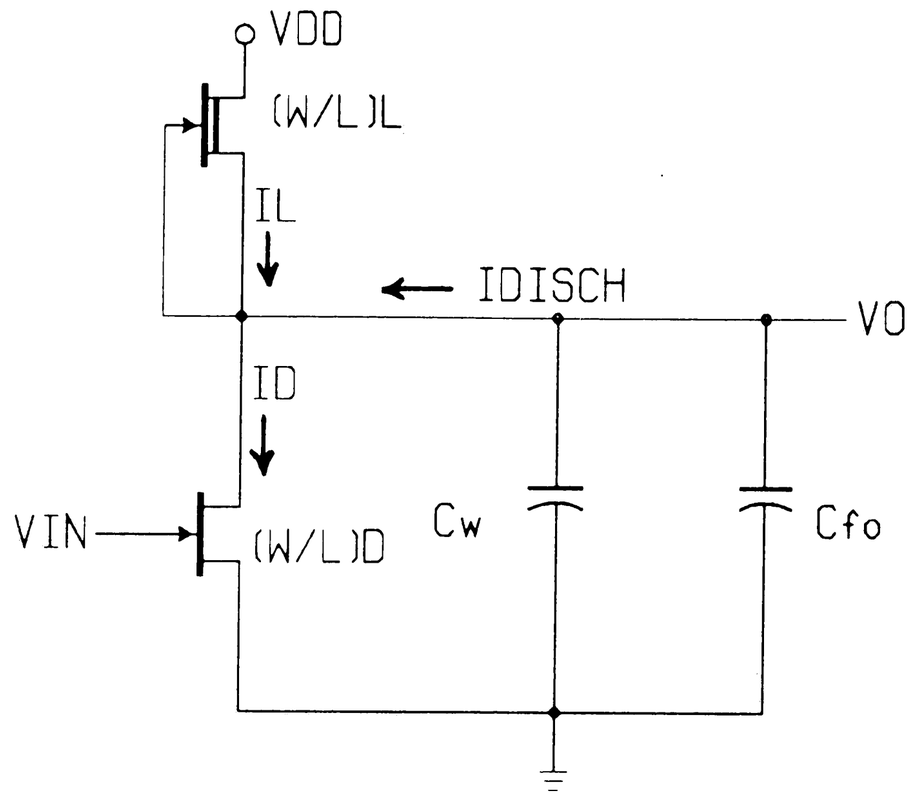


(a)



(b)

Figure 2.7. Charging Characteristics of DCFL Inverter.



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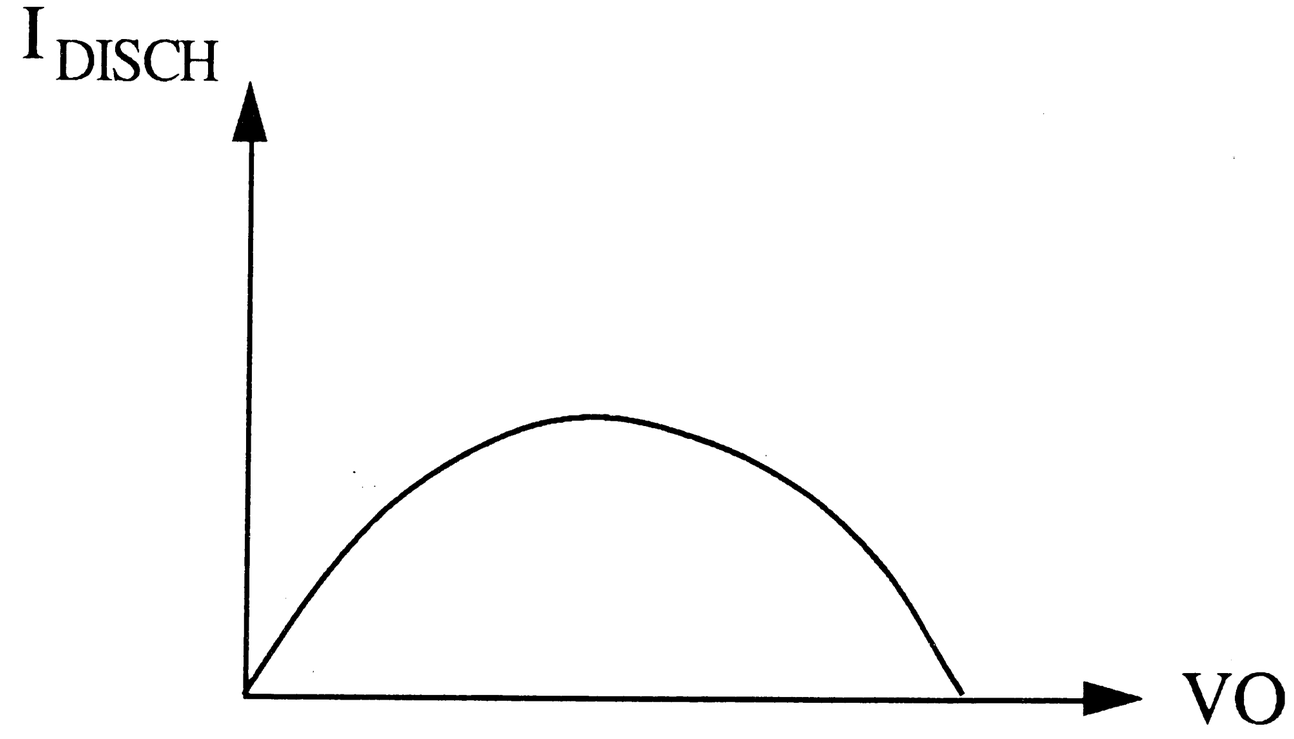


(b)

Figure 2.8. Discharge Characteristics of DCFL Inverter.

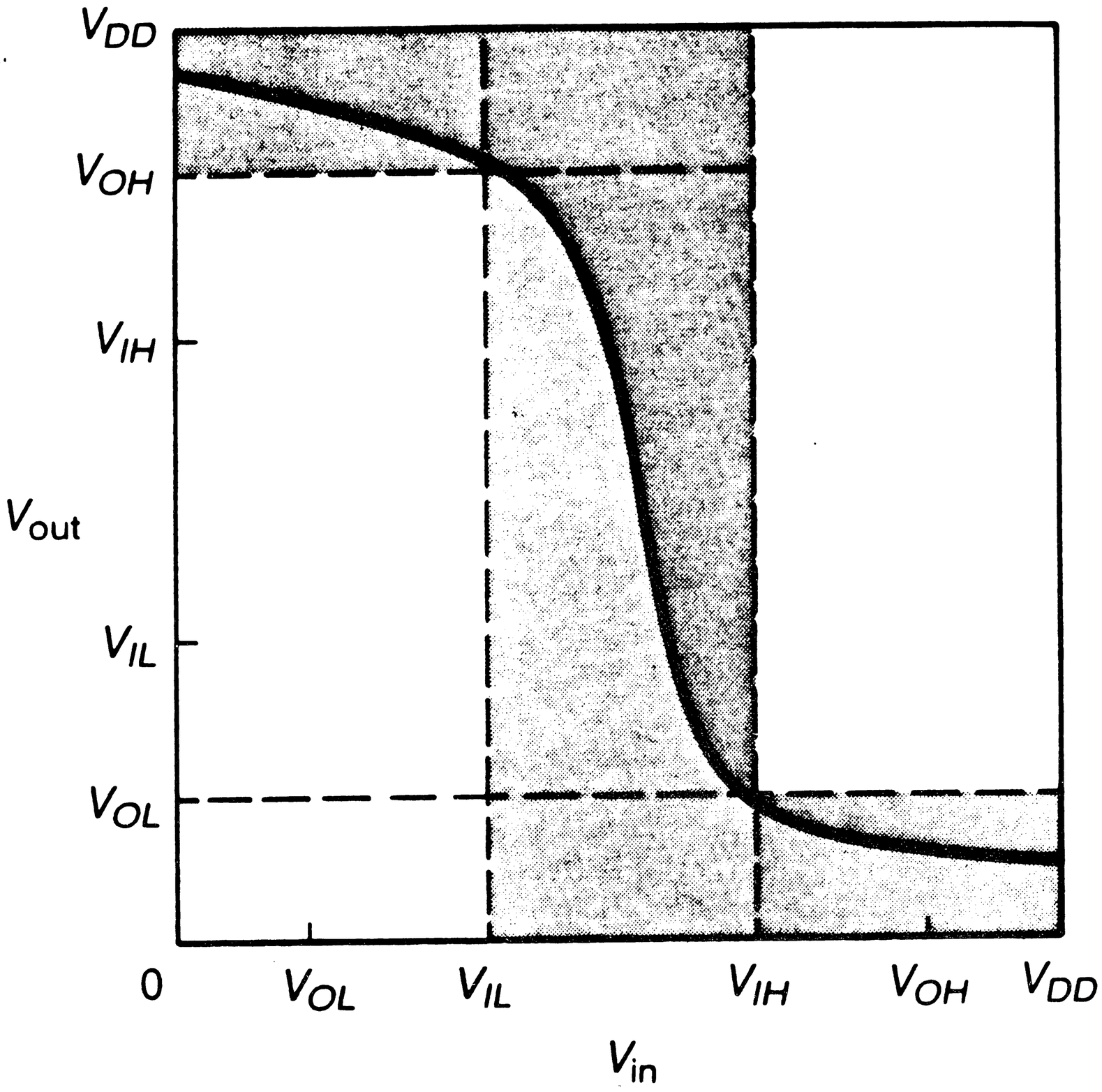


Figure 2.9. Inverter DC Transfer Curve (from ref. [3]).

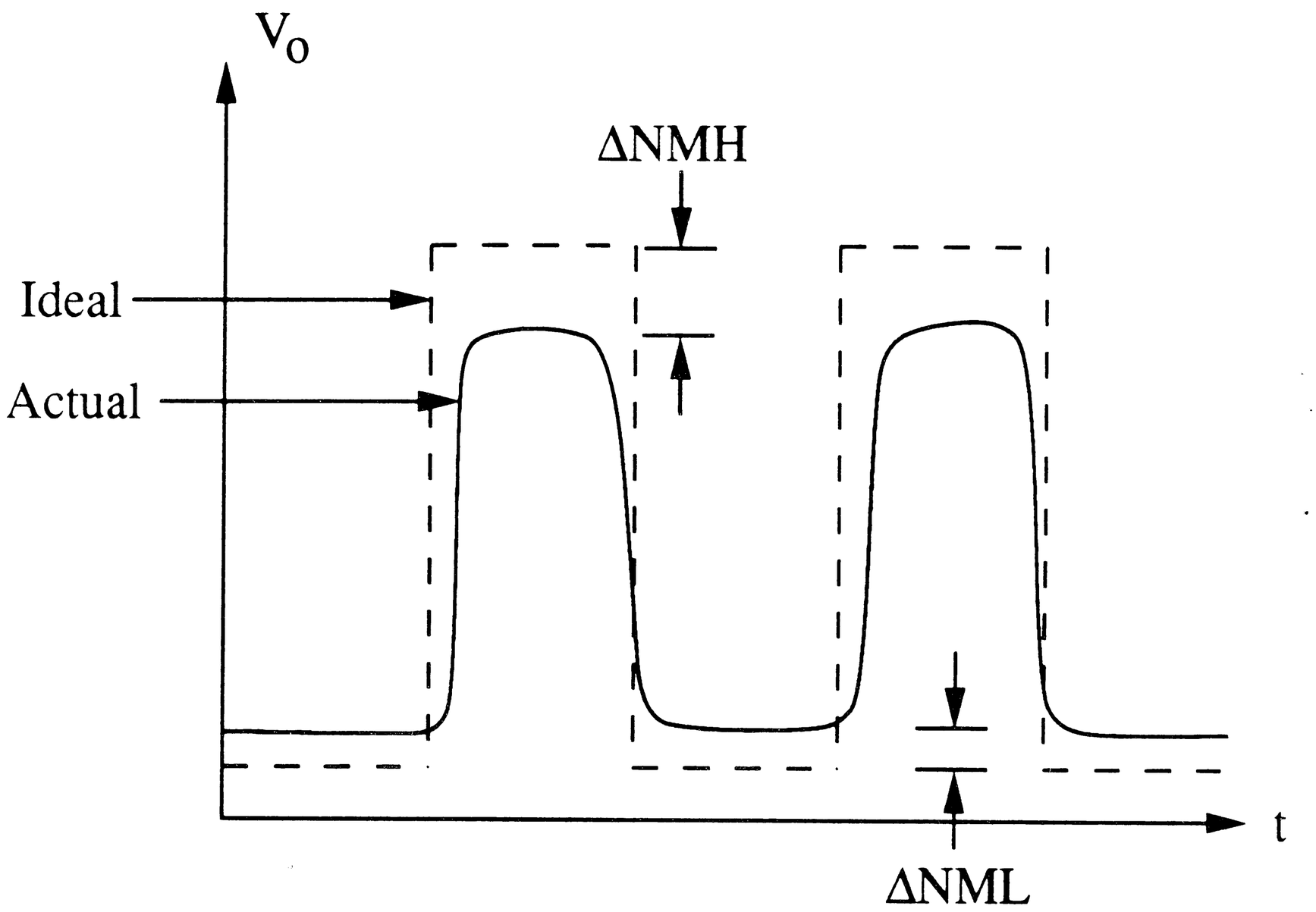


Figure 2.10. Inverter Transient Response Curve.

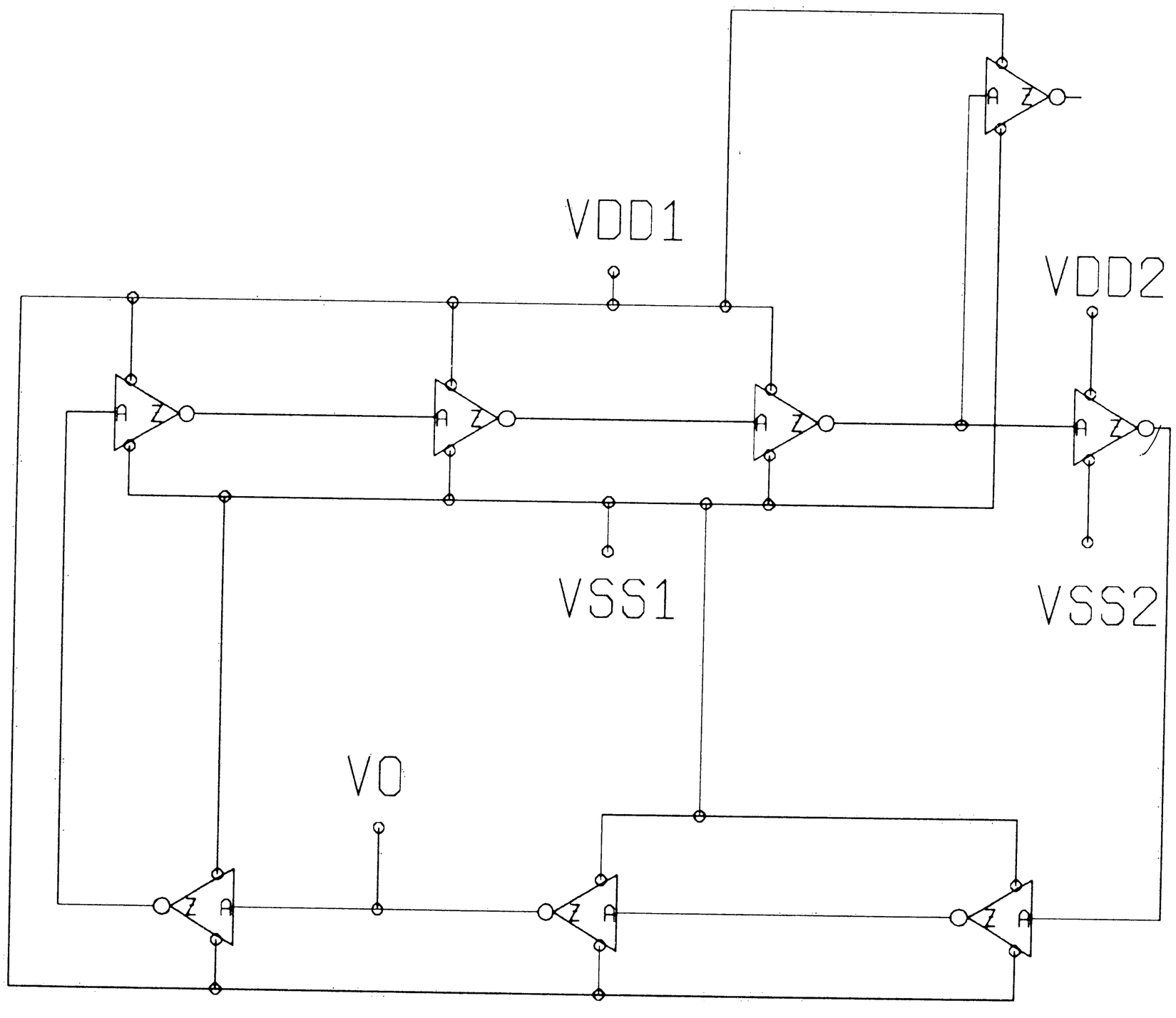


Figure 2.11. AC Noise Margin Measurement Set-up.

CHAPTER 3

HETRO-JUNCTION GaAs FET TECHNOLOGY

3.1. Physics of Hetro-junction FETs (HFET)

AT&Ts' digital GaAs technology is based on a Molecular Beam Epitaxy (MBE) grown Hetero-junction Field Effect Transistor (HFET), which is also known as a HEMT, MODFET, and TEGFET by various vendors. The HFET is a modulation doped FET formed by selective doping of GaAs and AlGaAs layers as shown in Figure 3.1. The HFET has recently emerged to demonstrate the realization of very fast switching gates. Propagation delays for DCFL ring oscillators as low as 10 pS at 300° K have been reported [9].

The HFET uses a high mobility and high velocity two-Dimensional Electron Gas (2 DEG) formed at the AlGaAs-GaAs interface to conduct current. This results in carrier confinement to reduce ionized impurity scattering and maintain a constant depletion layer width. Since the depletion layer in an HFET is constant, a higher constant transconductance can be achieved with a higher drain current per unit width over the MESFET. This section will present a basic formulation for quantifying the 2 DEG, followed by the charge control model, and then the current/capacitance characteristics of the HFET.

3.1.1 2 DEG Quantization

Understanding of HFET device operation is gained by quantifying the 2 DEG in the channel. This analysis parallels the analysis performed on calculating the inversion layer carrier density in silicon MOS devices.

When a doped AlGaAs layer is grown on top of an undoped GaAs layer a 2 DEG is formed at the interface due to the conduction band discontinuity as shown in Figure 3.1. The 2 DEG gas is quantized in a direction perpendicular to the hetro-interface. The 2 DEG motion can be characterized by an envelope function (see Equation 3.1) using the effective mass approximation as derived by F. Stern for n-type silicon inversion layers in MOS devices [6].

$$F(x,y,z) = \Phi(z)\exp(iQ\bullet R) \qquad (3.1)$$

where Q is a 2D wave vector for motion parallel to the hetro-interface, R is a 2D vector in the interface plane, and z is the distance into the undoped GaAs layer from the interface. The $\phi(z)$ wave function satisfies Shrodinger's equation:

$$\frac{\hbar^2}{2m}\frac{d^2\phi_i}{dz^2} + [E_i - V(z)]\,\phi_i = 0 \qquad (3.2)$$

where m is the electron effective mass in a bulk GaAs conduction band, E_i is the ith subband quantized energy level, and V(z) band bending potential energy at the

interface. Solving for V(z) using Poisson's equation under boundary conditions under which free electrons are confined to the channel of $\phi(\infty) = 0$ and $\phi(-\infty) = 0$:

$$\frac{d^2V(z)}{dz^2} = q\,\rho(z)/\varepsilon \qquad (3.3)$$

$\rho(z)$ is the space charge density in the GaAs which is the sum of conduction band electrons and ionized acceptor (N_A^-) and donor (N_D^+) densities. $\rho(z)$ can be expressed as:

$$\rho(z) = q\,(N_D^+ - N_A^-) - q\sum_{i=0}^{\alpha} n_i\,|\phi_i|^2_{(z)} \qquad (3.4)$$

$$n_i = \left(\frac{m\,k_B\,T}{\hbar^2}\right) \ln\left[\,1 + EXP\left[\,q\,(E_F - E_i\,)/\,k_B T\right]\right] \qquad (3.5)$$

Using a triangular well approximation, the potential energy near the interface can be approximated:

$$V(z) = q\,F_s\,z \qquad (3.6)$$

where F_S is the surface electric field. The solution leads to the Airy equation for subband energies [4]:

$$E_i = \left(\frac{\hbar^2}{2\,m}\right)^{\frac{1}{3}}\left[\,3\,q\,F_s\,\pi\left(i + \frac{3}{4}\right)\right]^{\frac{2}{3}} \qquad (3.7)$$

Gauss's law relates the surface field Fs to the carrier density n_s:

$$n_s = \frac{1}{q} E F_s \qquad (3.8)$$

where

$$n_s = \sum_{i=0}^{\alpha} n_i \qquad (3.9)$$

Substitution of Equation (3.9) into Equation (3.7) yields the subbands energy levels E_0 and E_1 :

$$E_0 = \gamma_0 (n_s)^{\frac{2}{3}} \qquad (3.10)$$

$$E_1 = \gamma_1 (n_s)^{\frac{2}{3}} \qquad (3.11)$$

γ_0 and γ_1 are estimated from cyclotron resonance data [6]:

$$\gamma_0 = 2.5 \times 10^{-12} \, v \, m^{\frac{4}{3}}$$
$$\gamma_1 = 3.2 \times 10^{-12} \, v \, m^{\frac{4}{3}} \qquad (3.12)$$

Consideration of the first 2 subband energy leads to satisfactory engineering results [7] for carrier concentration n_s:

$$n_s = \frac{D\,k\,T}{q} \sum_{i=0}^{1} \ln\,[\,1 + EXP\,[\,q\,(E_F - E_i)/kT\,]\,] \qquad (\ 3.13\ )$$

where D is the density of states for the 2 DEG as determined by cyclotron effective mass measurement.

$$D = 3.24 \times 10^{17}\ m^{-2}\ v^{-1} \qquad (\ 3.14\ )$$

3.1.2 Charge Control

In this section, the necessary equations for developing the drain current control of an HFET device will be stated. The analysis starts by quantifying the channel electron density n_s as a function of the gate-to-source voltage.

When a Schottky gate contact is placed on AlGaAs, charge control of the 2 DEG can be achieved. When a large gate to source voltage is applied, the AlGaAs region will deplete as shown in Figure 3.2.

The carrier concentration n_s of the 2 DEG is given by [7]:

$$n_s = \frac{\varepsilon}{q\,d}\,[V_g - (\phi_b\,V_{p2} + V(di^+) - \Delta E_C \qquad (\ 3.15\ )$$

where Vg is the applied gate voltage, ϕ_b is Schottky barrier height, $V(di^+)$ is the voltage across the undoped AlGaAs layer and V_{p2} is pinch-off voltage of the doped AlGaAs:

$$V_{p2} = \frac{q\, N_D\, d_d^2}{2\varepsilon} \qquad (3.16)$$

d_d is the total thickness of the doped AlGaAs beneath the gate and $d = d_d + d_i$. A relationship between $V(d_i+)$ and n_s can be approximated and is shown in Figure 3.3 [12].

$$V(d_i^+) = \Delta E_{F0}(T) + a\, T \qquad (3.17)$$

where $a = 0.125 \times 10^{-16}$ Vm^2, and $\Delta E_{f0} \approx 0$ at 300° K and 0.025 V at 77° K and below. Thus, the charge control model can be written as:

$$n_s = \frac{\varepsilon}{q\,(d + \Delta d)}\,(V_g - V_{OFF}) \qquad (3.18)$$

$$V_{OFF} = V_{OFF}' + \Delta E_{F0} \qquad (3.19)$$

$$V_{OFF}' = \phi_b - \Delta E_C - V_{p2} \qquad (3.20)$$

$$\Delta d = \frac{\varepsilon\, a}{q} \approx 80\ \text{Å} \qquad (3.21)$$

where Δd is a correction factor for Enhancement devices. Figure 3.3 compares the exact solution versus the approximate solution.

3.1.3 Current/Capacitance-Voltage Characteristics

The current characteristics of HFET devices have been derived by Michael S. Shur [8] and Park and Kwack [9]. The derivation by Shur is a piece-wise linear approximation for the field velocity characteristics as shown in Figure 3.4.

The Park and Kwack derivation is a closed form derivation which is more suitable for computer simulation of HFET integrated circuits. Their derivation starts with the charge control model and current density equation, the device energy band diagram is shown in Figure 3.5 and an equivalent circuit model is shown in Figure 3.6. When a gate bias is applied:

$$n_s = \frac{\varepsilon_1}{q\,d}\,(V_g - V_{OFF}) \qquad (3.22)$$

The voltage needed to deplete the doped AlGaAs entirely is:

$$V_p = -\frac{q\,N_D\,(d_d + di - w_1^2)}{2\varepsilon_1} \qquad (3.23)$$

$$Q_s = q\,n_s = \frac{\varepsilon_1}{d}\,(V_g - V_{OFF}) \qquad (3.24)$$

$$I = -W\left[\,\mu\,E_z\,Q_s + D_n\,\frac{dQ_s}{dz}\,\right] \qquad (3.25)$$

For the linear region the drain current can be derived to give [10]:

$$I = \frac{E_s L}{4 R_s}\left[\left(\frac{V_o}{E_s L} + 2\alpha\beta R_s - \alpha R_s V_D + 1\right)\right. \qquad (3.26)$$

$$\left. - \sqrt{\left(\frac{V_D}{E_s L} + 2\alpha\beta R_s - \alpha R_s V_D + 1\right)^2 - \frac{8\alpha R_s}{E_s L}\left(\beta V_D - \frac{V_D^2}{2}\right)}\right]$$

where

$$\alpha = \frac{W \mu_0 \varepsilon_1}{d L} \qquad (3.27)$$

$$\beta = V_g - V_{OFF} + \frac{k T}{q}$$

In saturation the derivation starts with Poisson's equation:

$$\frac{d^2 V}{dz^2} = \frac{\rho}{\varepsilon_2} = \frac{1}{\varepsilon_2}\frac{J}{v_s} \qquad (3.28)$$

$$J = \frac{I_s}{W d_0} \qquad (3.29)$$

where v_s is carrier drift velocity and I_S is saturation current, under the boundary conditions of:

$$V(z=0) = V_{DS} - R_d I_s \,,\; R_d = R_s \qquad (3.30)$$

$$V(z=\Delta L) = V_D - R_d I_s \,,\; R_d = R_s \qquad (3.31)$$

where V_{DS} is the saturation drain to source voltage, R_S and R_D are the source and drain resistances, d_0 is the 2 DEG layer width and ΔL is the reduced channel length when $V_D > V_{DS}$.

The current-voltage characteristics can then be represented by:

$$V_D = V_{DS} + \frac{I_s L^2}{2 W d_0 \varepsilon_2 v_s}\left(1 - \frac{I_{DS}}{I_s}\right)^2 - E_s L\left(1 - \frac{I_{DS}}{I_s}\right) \qquad (3.31)$$

The capacitance-voltage characteristics have been derived by Shur [8]. Using this model the gate-source capacitance Cgs and gate-drain capacitance Cgd are as follows:

$$Q_T = W \int_0^L q\, n_s\, dz \qquad (3.32)$$

$$Q_T = W \int_{V_s}^{V_D} q\, n_s \frac{dz}{dV}\, dV \qquad (3.33)$$

$$Q_T = \frac{2}{3} C_0 \frac{V_{gs}^3 - V_{gd}^3}{V_{gs}^2 - V_{gd}^2}\ , \quad C_0 = \frac{\varepsilon W}{d + \Delta d} \qquad (3.34)$$

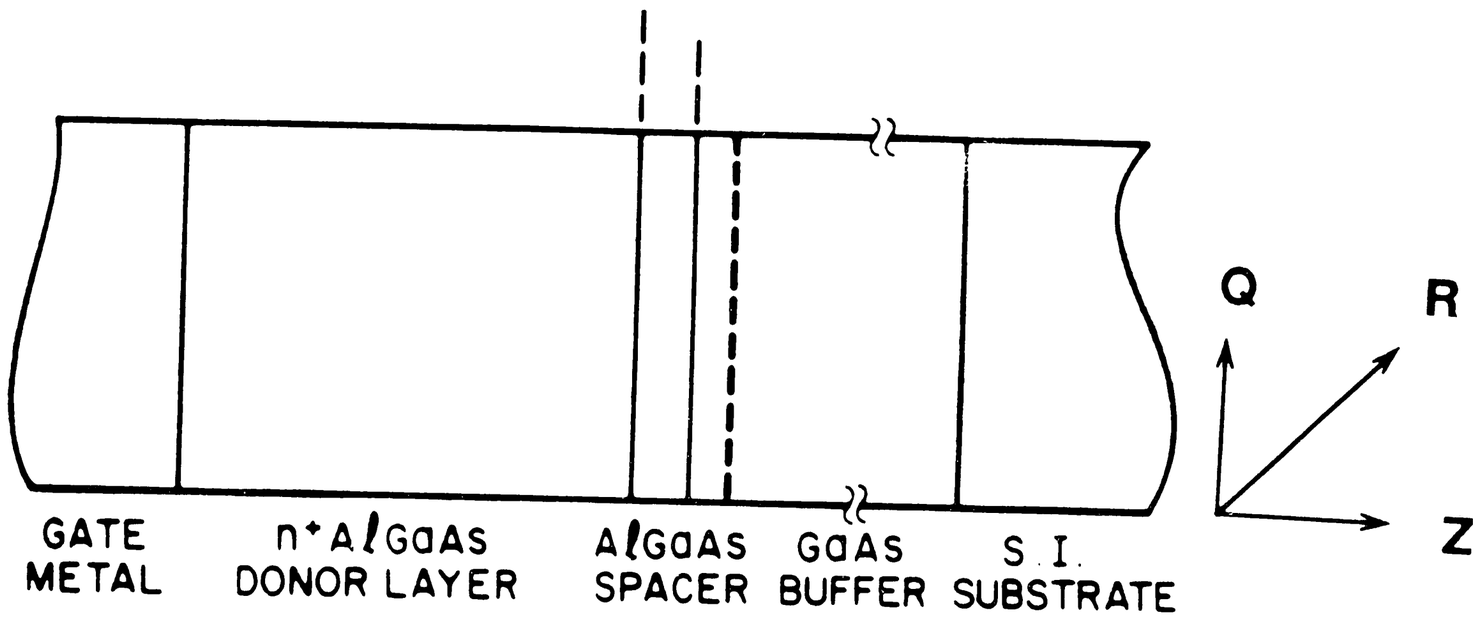
Then

$$C_{gs} = \frac{dQ_T}{dV_{gs}} = \frac{2}{3} \frac{C_0 V_{gs} (V_{gs} + 2 V_{gd})}{(V_{gs} + V_{gd})^2} \qquad (3.35)$$

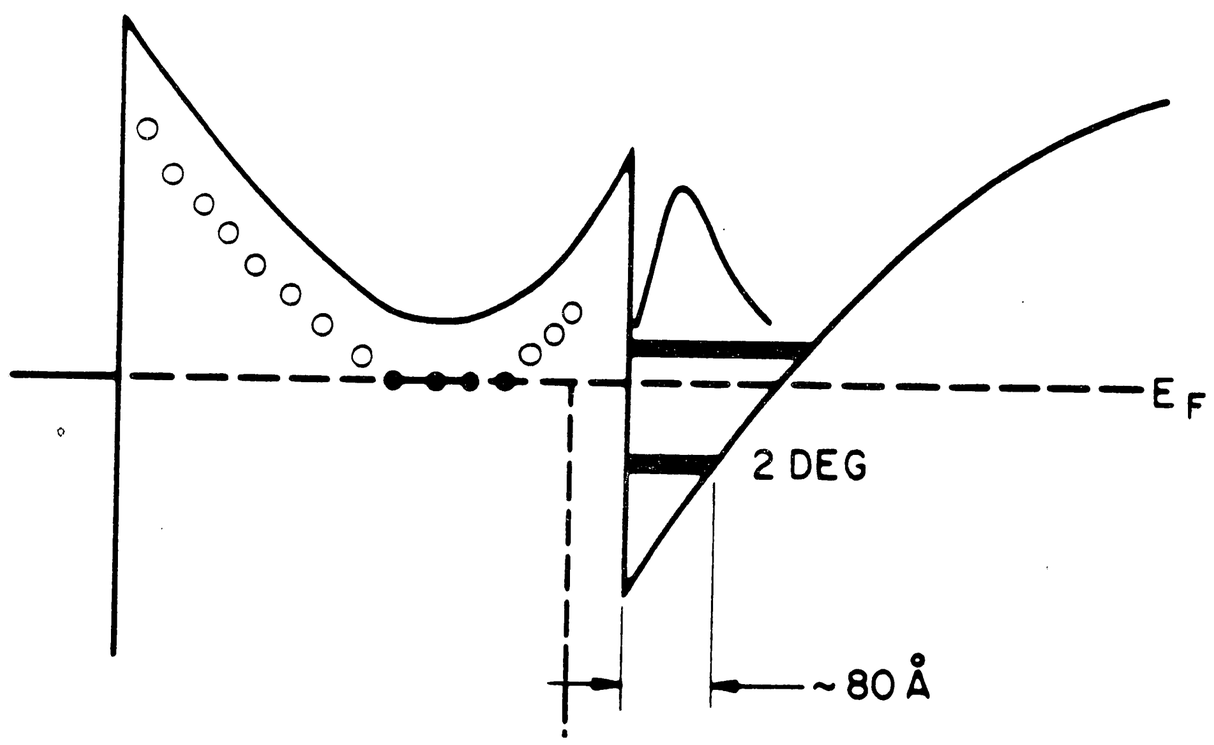
$$C_{gd} = \frac{dQ_T}{dV_{gd}} = \frac{2}{3} \frac{V_{gd} (V_{gd} + 2 V_{gs})}{(V_{gs} + V_{gd})^2} \qquad (3.36)$$

3.2. HFET Terminal Characteristics

This section shows the simulated HFET terminal characteristics using SargicS.13 model parameter set in AT&T's ADVICE circuit simulator. Also Schottky diode terminal characteristics are shown. Figures 3.7 to 3.10 show the EFET drain and gate characteristics at 25 and 125° C for nominal, high, and low current cases. Figure 3.11 show the EFET gate to source and gate to drain capacitances at 25 and 125° C. The DFET I-V characteristics are shown in Figures 3.12 to 3.15 for both 25 and 125° C temperatures for the nominal, high, and low current cases. Figure 3.16 shows the DFET gate to source and gate to drain capacitances at 25 and 125° C. Schottky diode characteristics are shown in Figures 3.17 and 3.18. The current and capacitance values shown in the figures are for a 1.0 μm wide device.



(a)



(b)

Figure 3.1. (a) HFET structure, (b) band diagram (from ref. [5]).

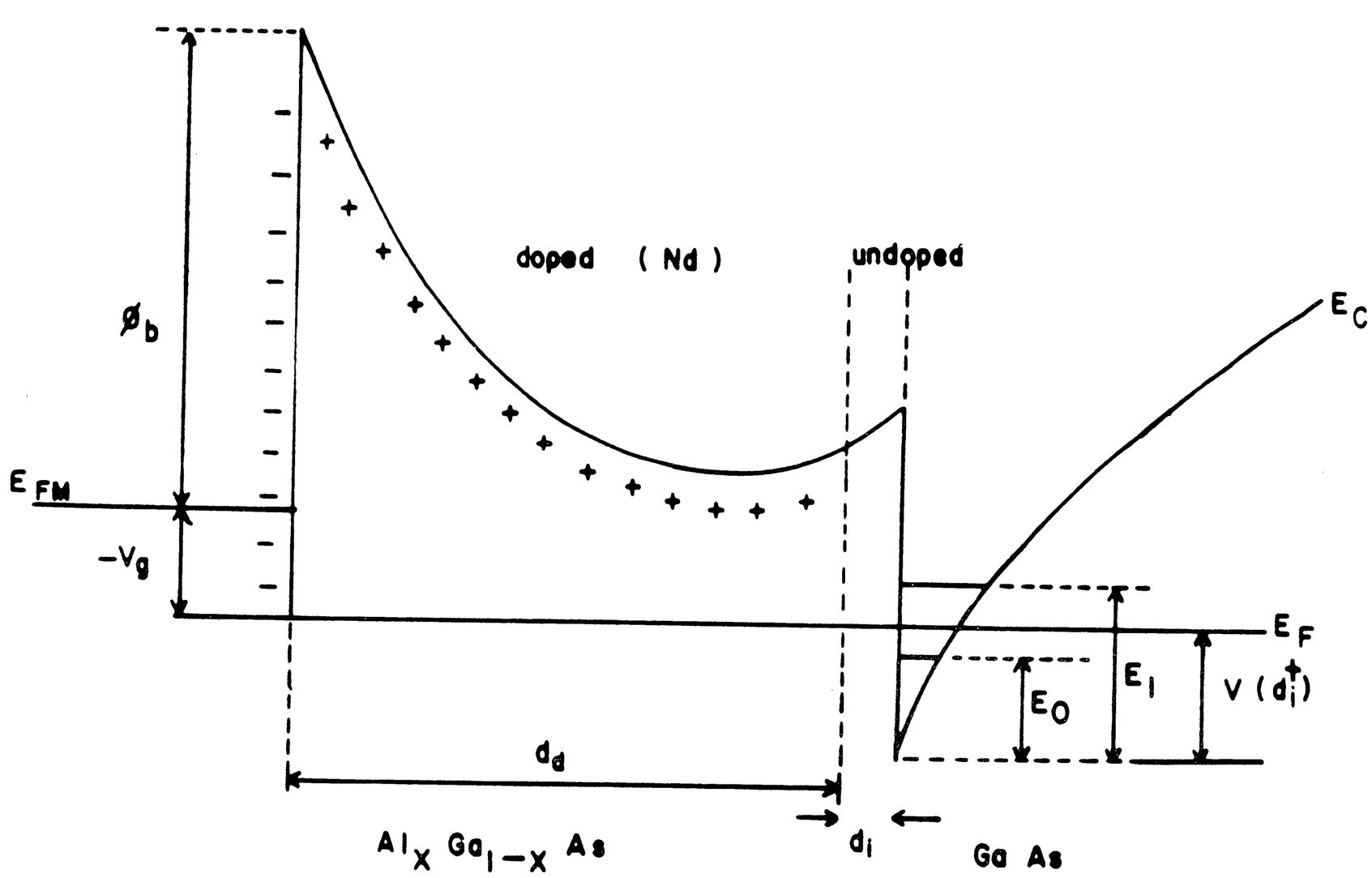


Figure 3.2. HFET Charge Control Model (from ref. [4]).

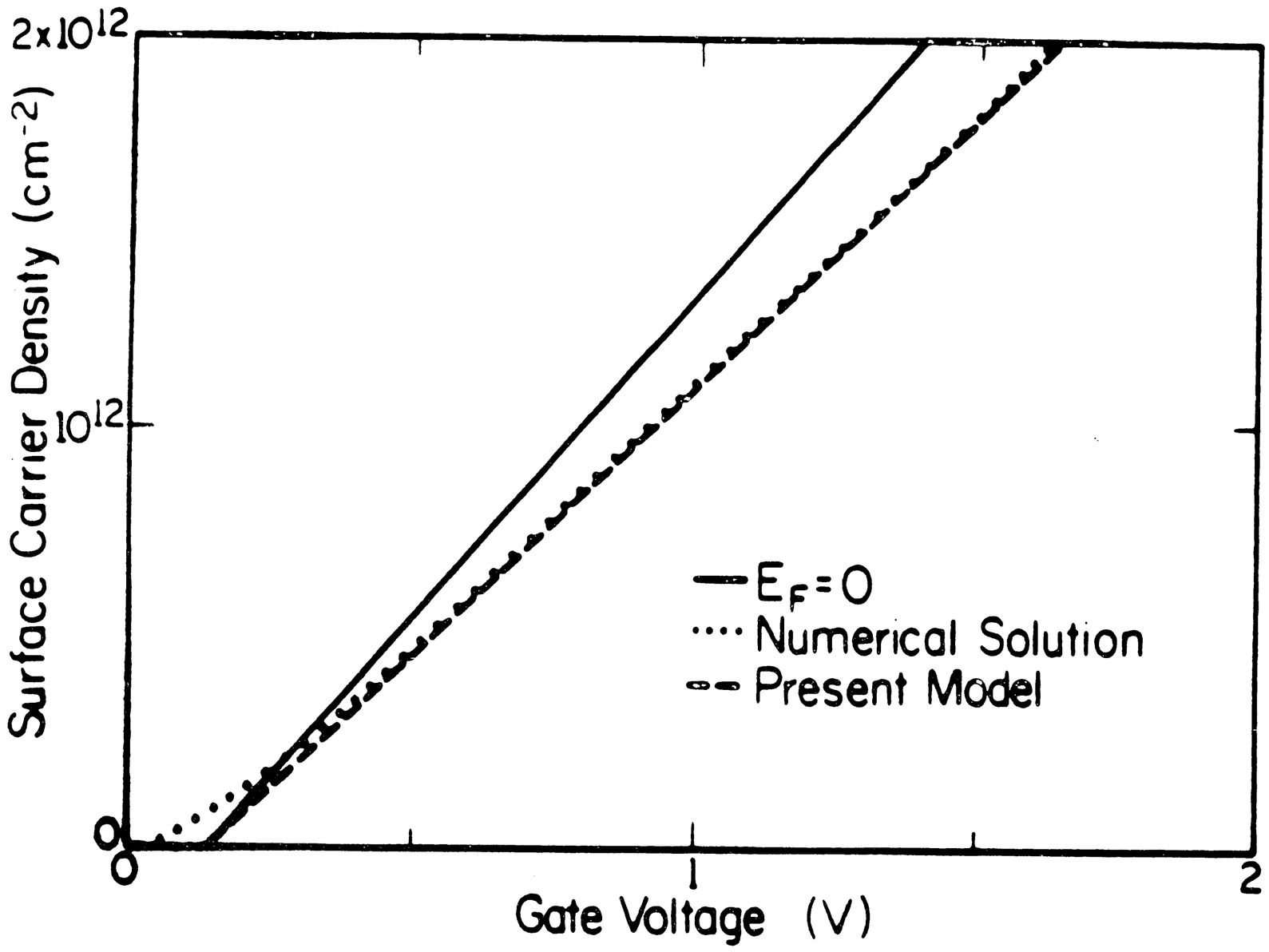


Figure 3.3. Surface carrier density versus gate voltage (from ref. [4]).

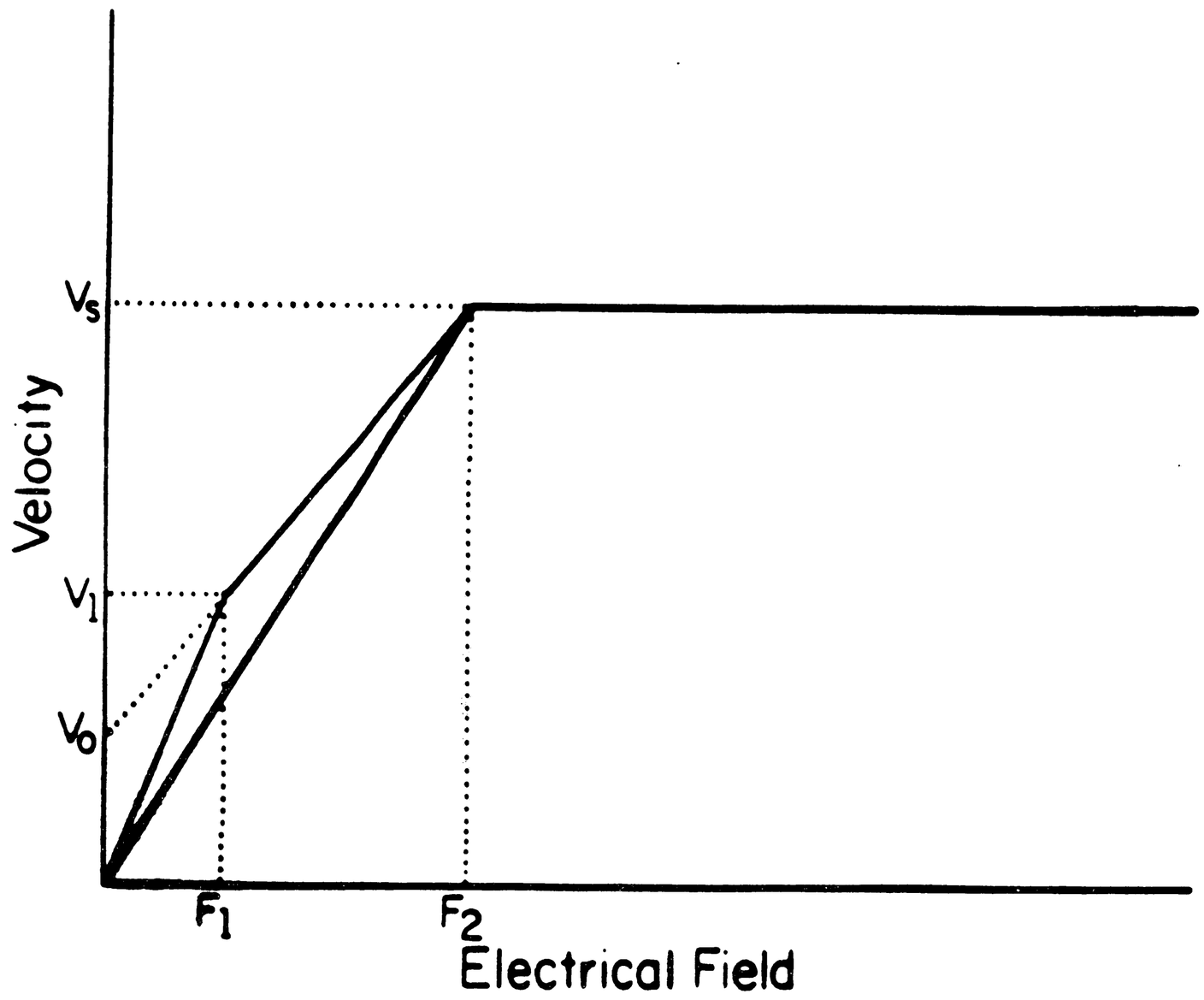


Figure 3.4. Two and three-piece linear approximation for velocity field characteristics (from ref. [7]).

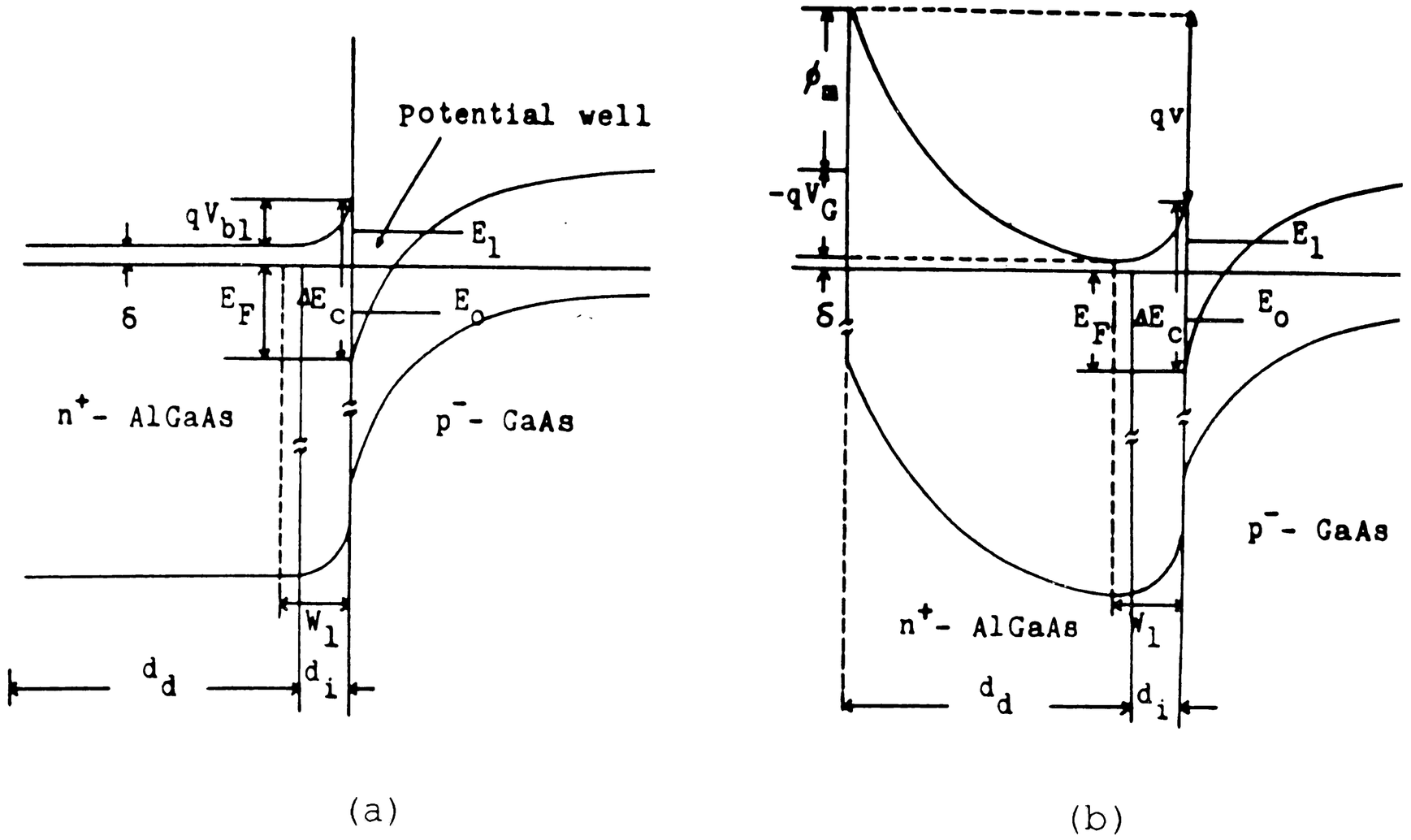


Figure 3.5. HFET energy band diagram (a) with no gate bias and (b) under gate bias (from ref. [10]).

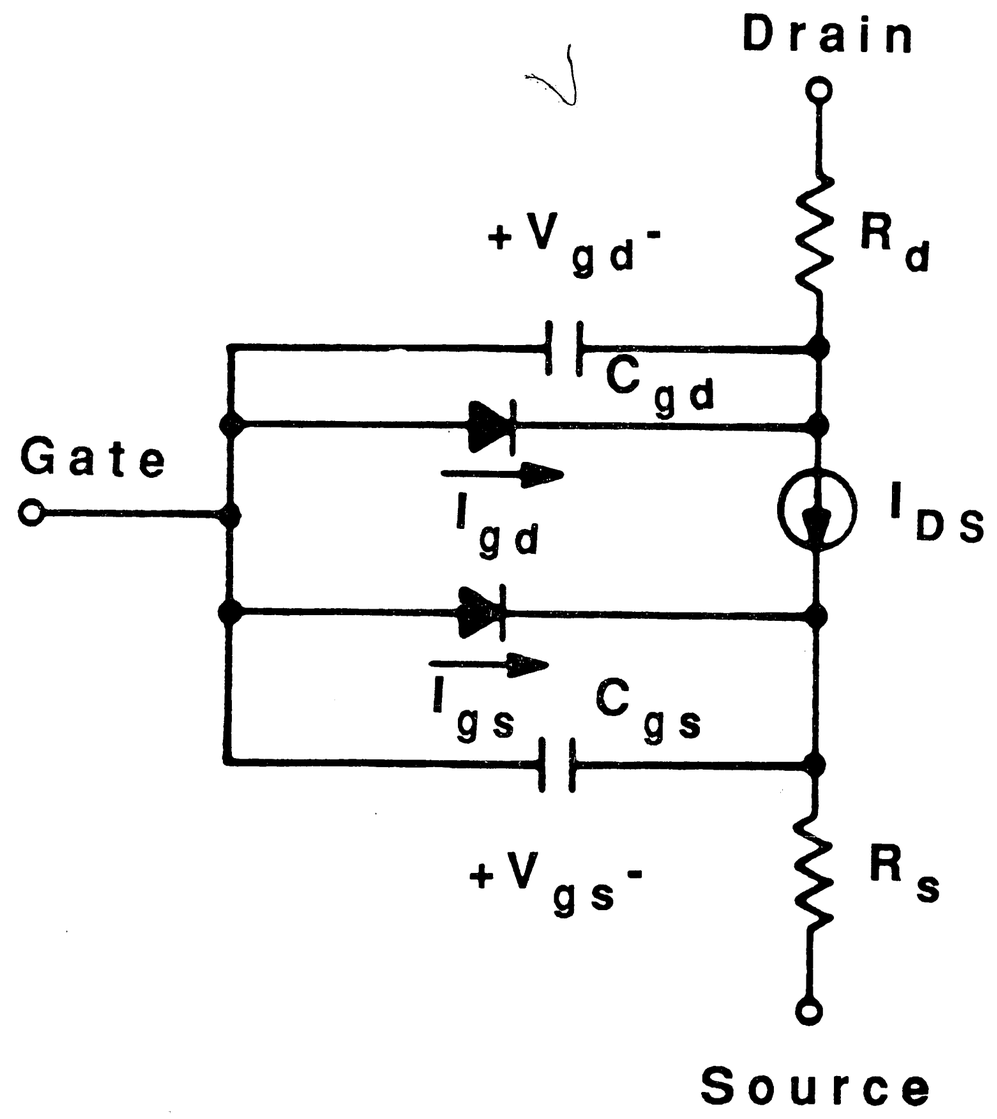


Figure 3.6. HFET equivalent circuit (from ref. [11]).

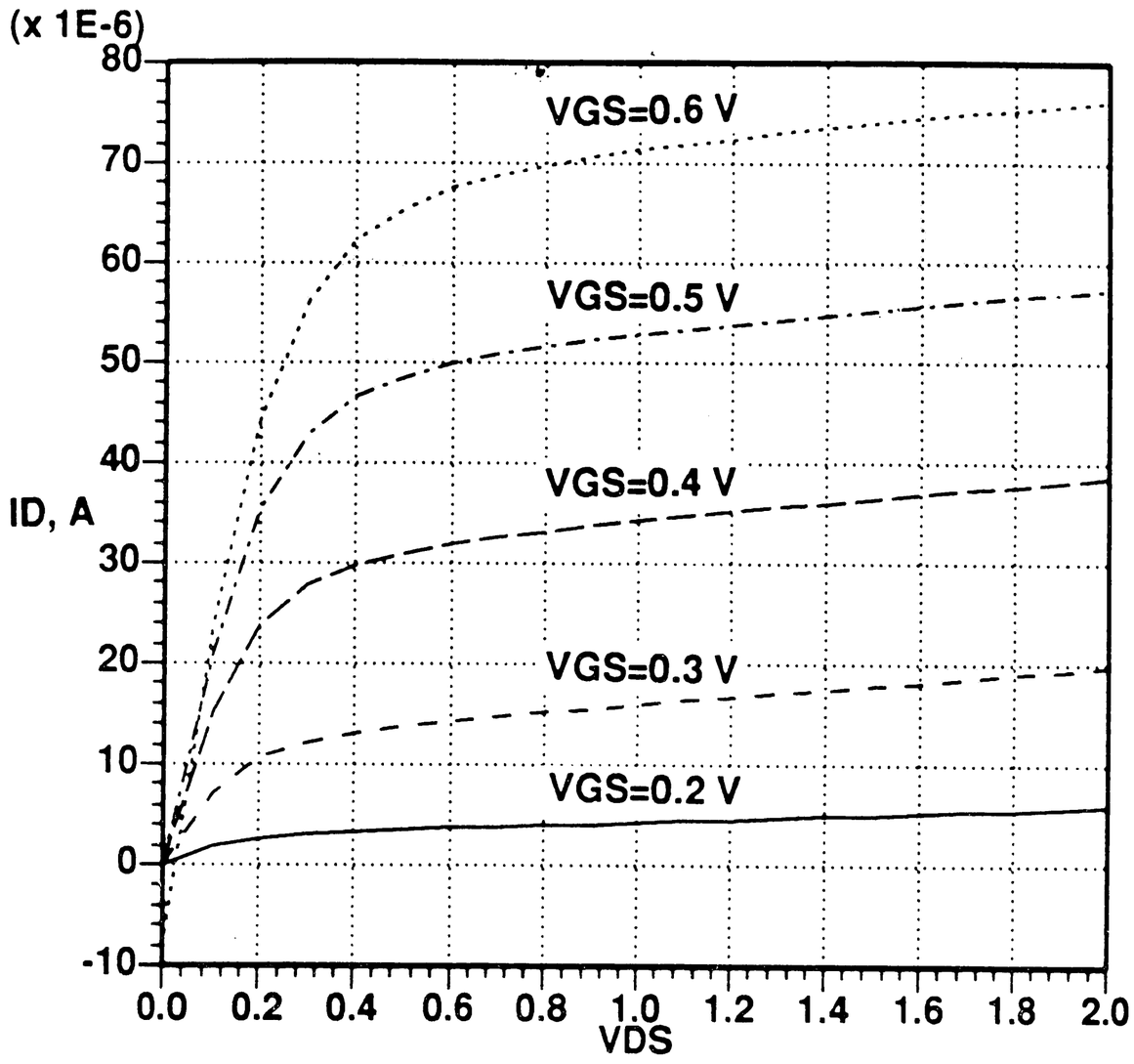


Figure 3.7. Nominal EFET IDS-VDS I/V curve characteristics at 25° C.

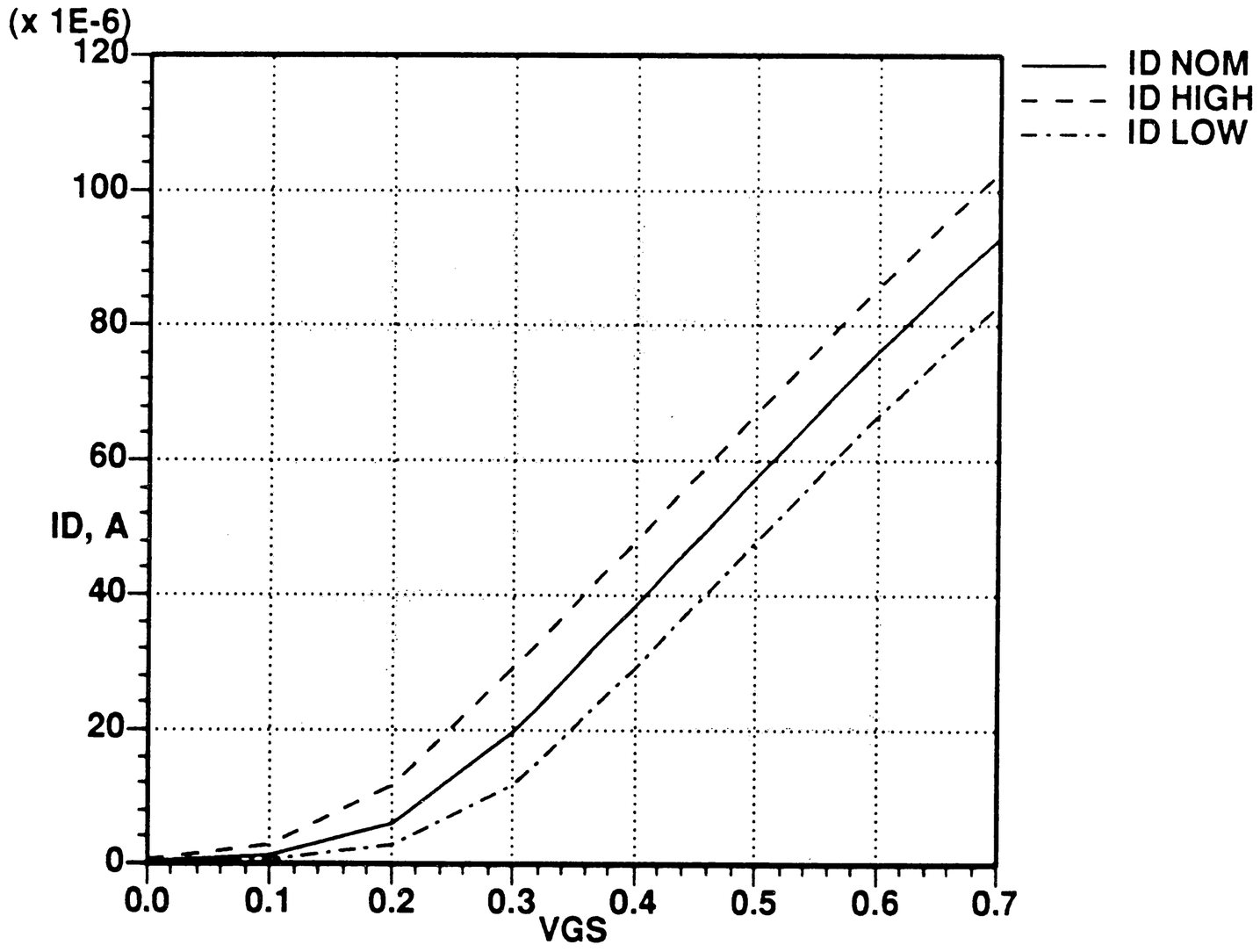


Figure 3.8. EFET IDS-VGS nominal, high, and low current characteristics at 25° C.

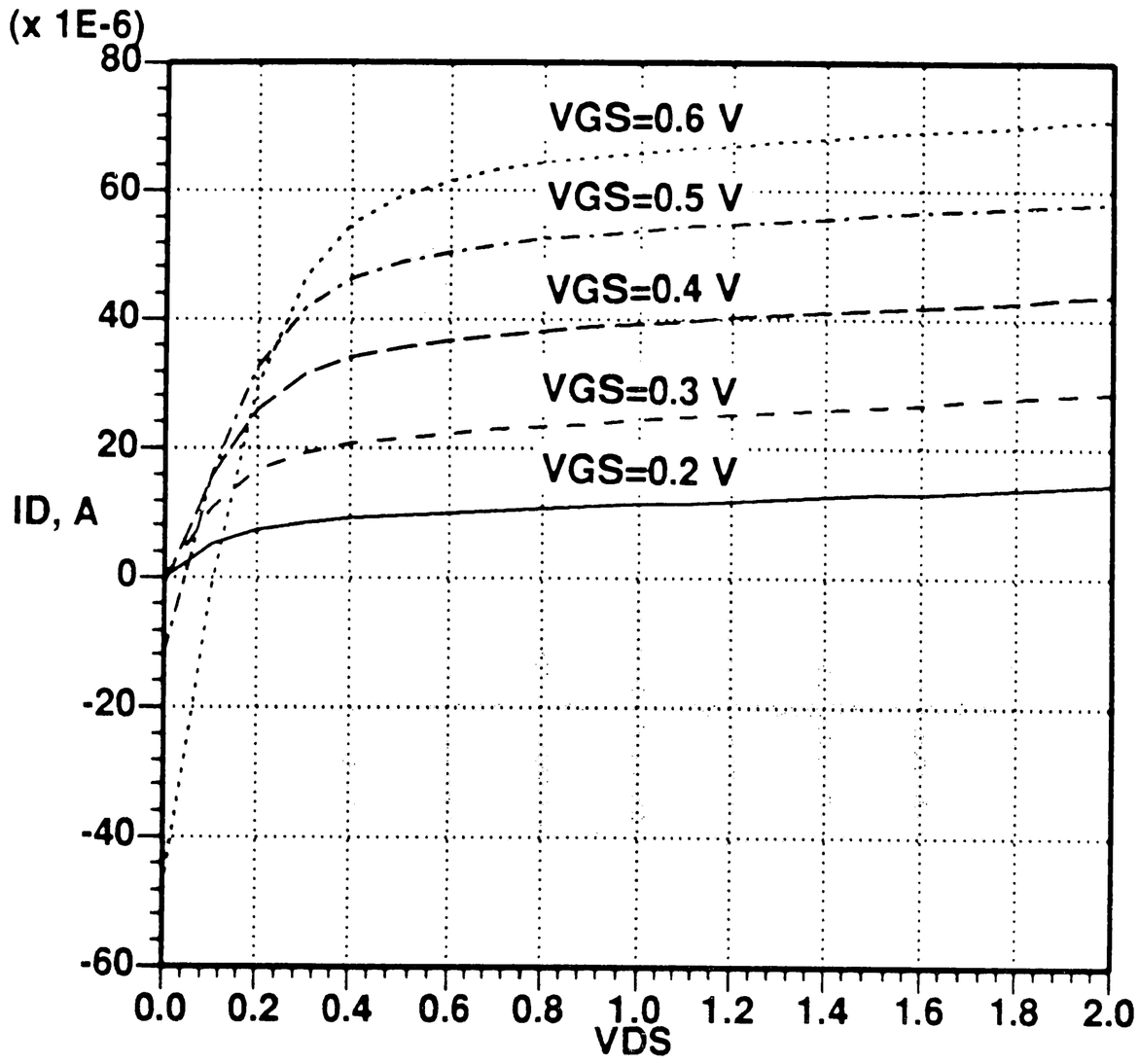


Figure 3.9. Nominal EFET IDS-VDS I/V characteristics at 125° C.

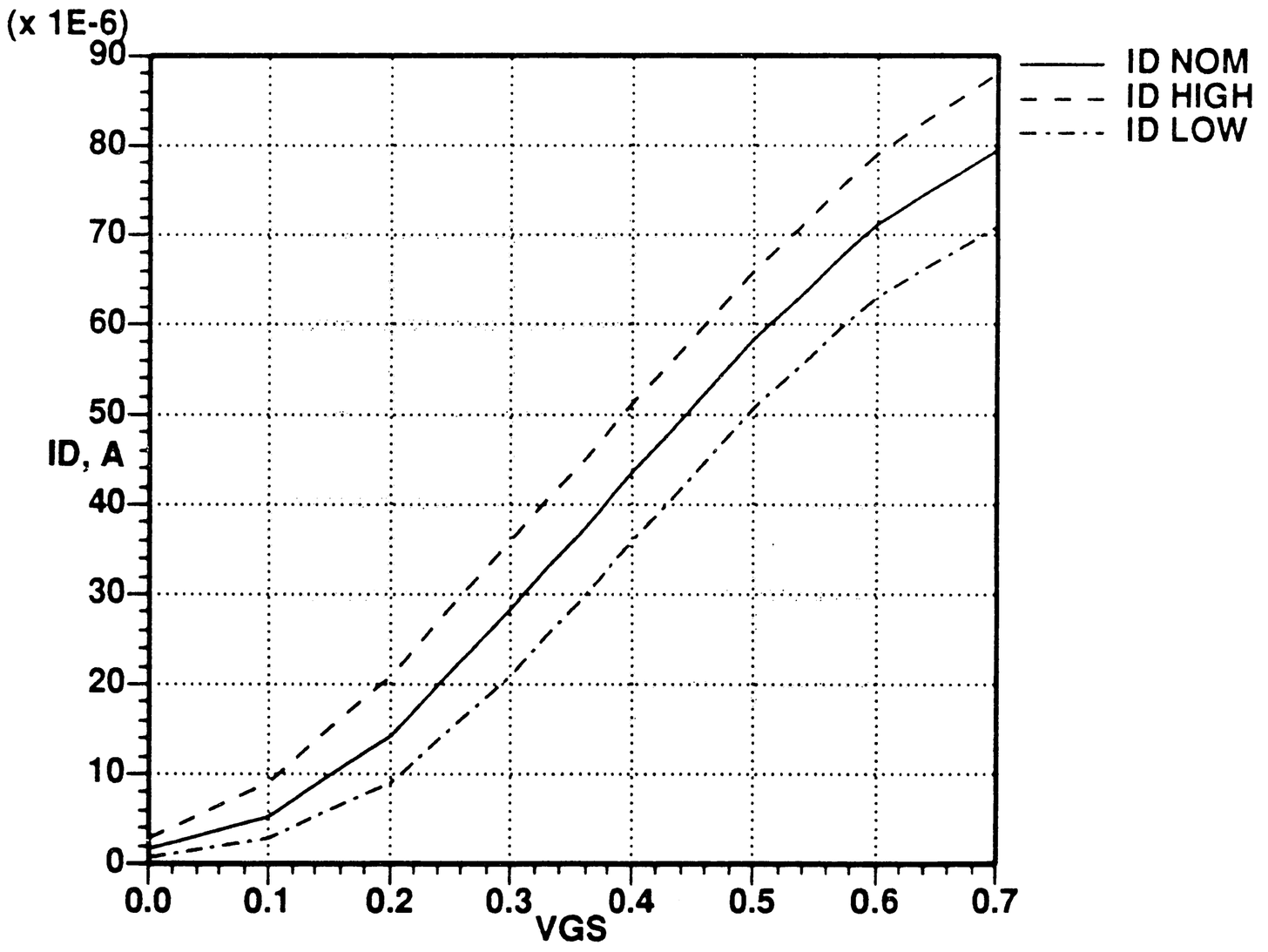


Figure 3.10. EFET IDS-VGS nominal, high, and low current characteristics at 125° C.

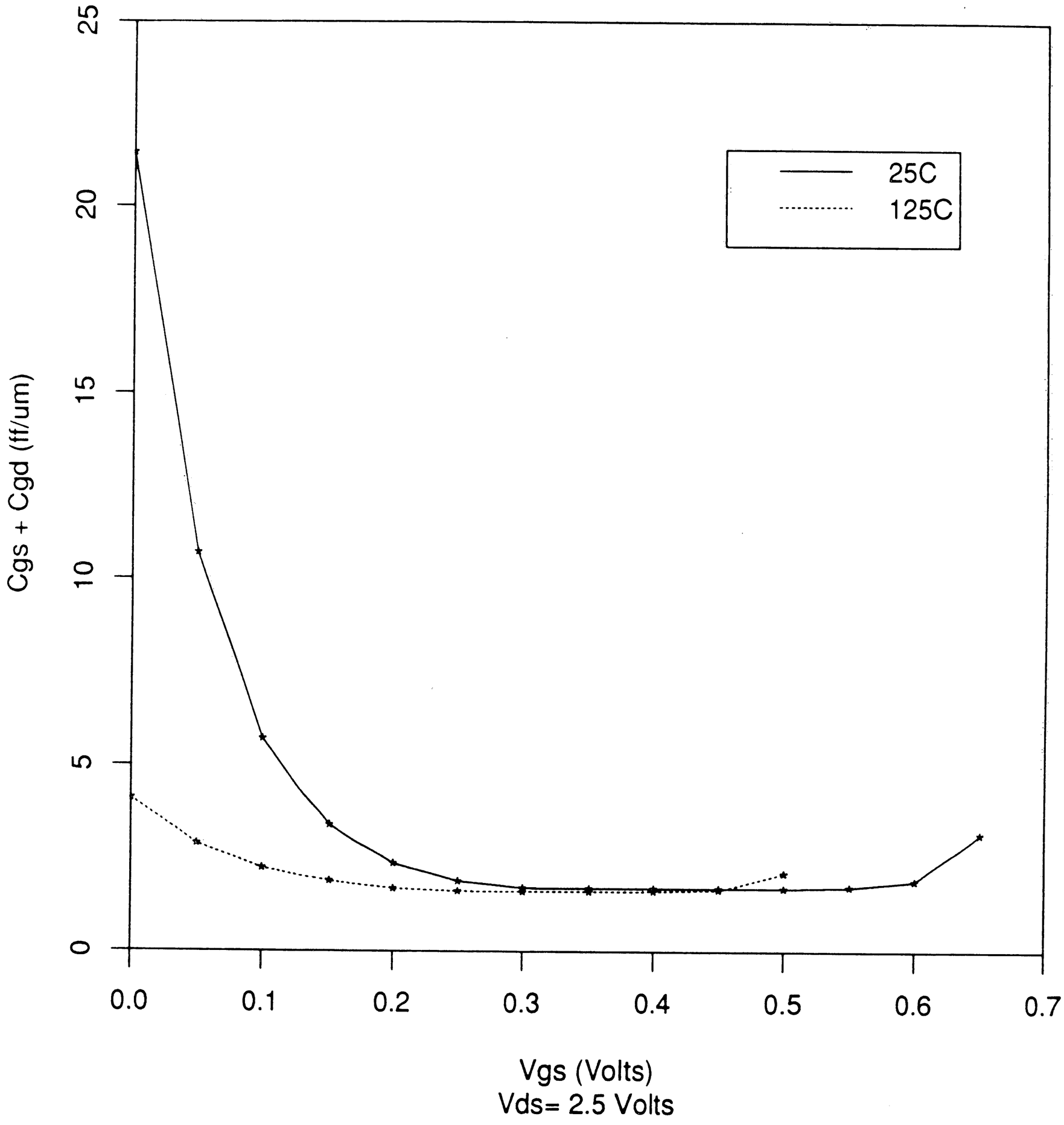


Figure 3.11. EFET Gate and drain-to-source capacitances Cgs and Cgd at 25° and 125° C.

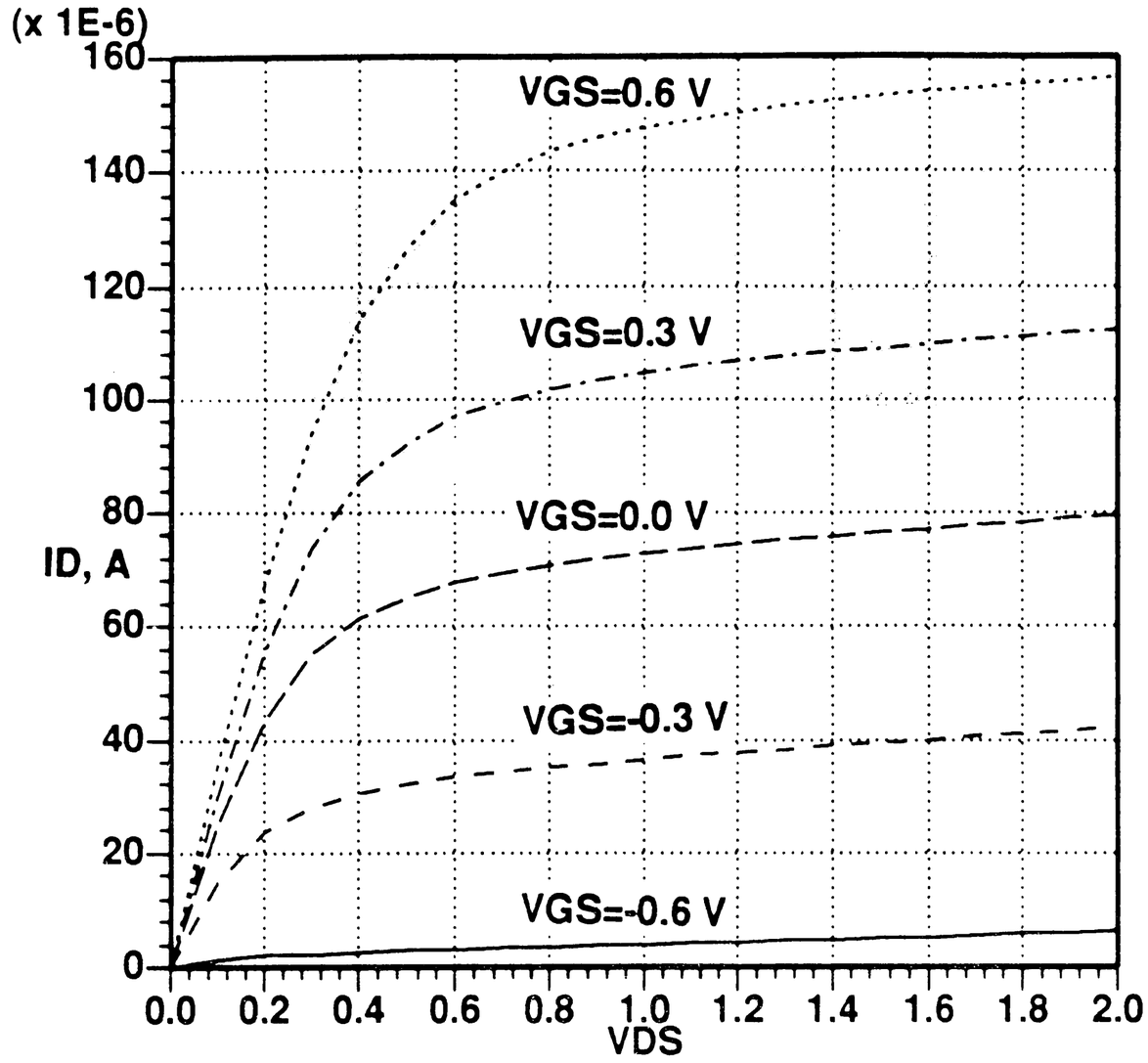


Figure 3.12. Nominal DFET IDS-VDS I/V characteristics at 25° C.

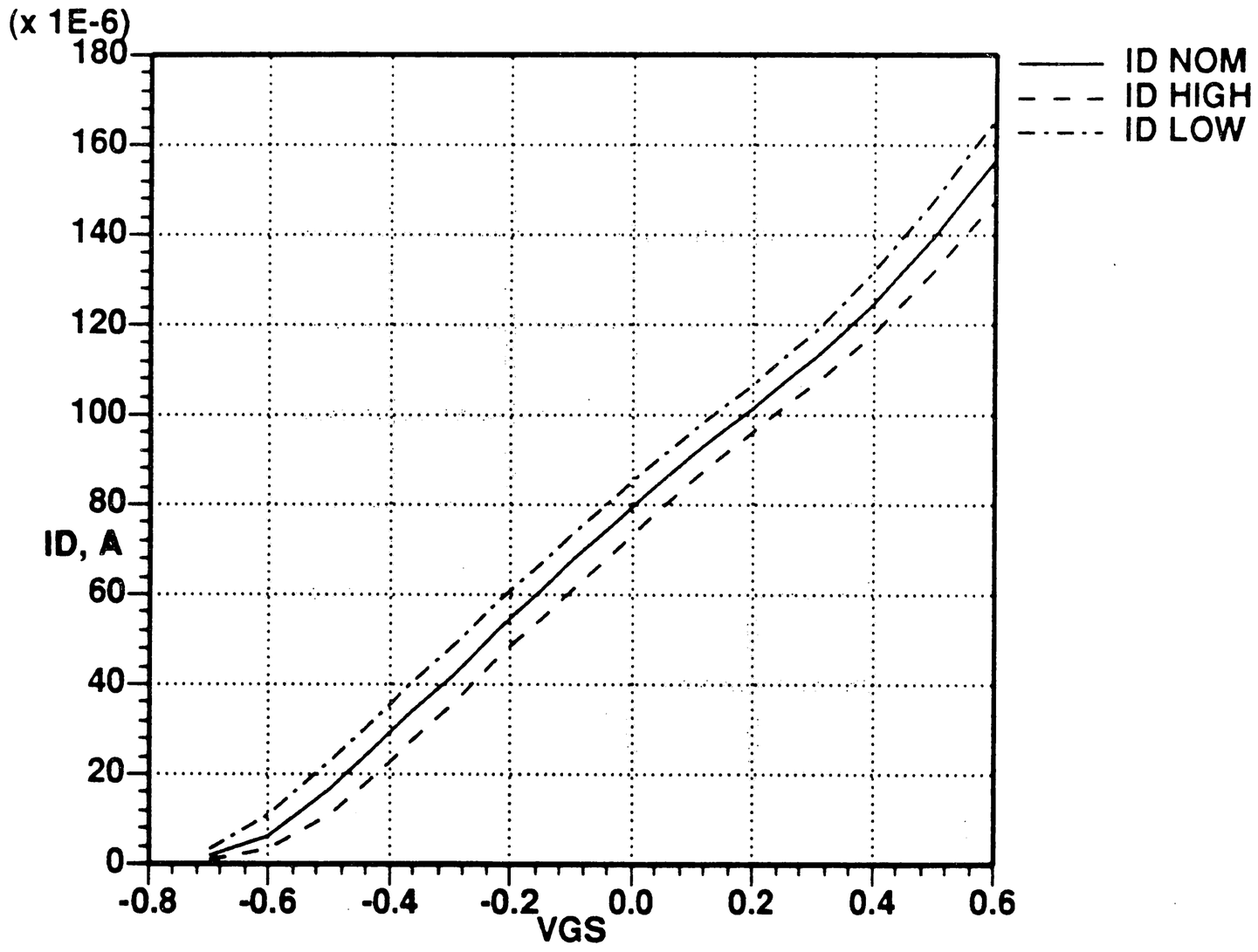


Figure 3.13. DFET IDS-VGS nominal, high, and low current characteristics at 25° C.

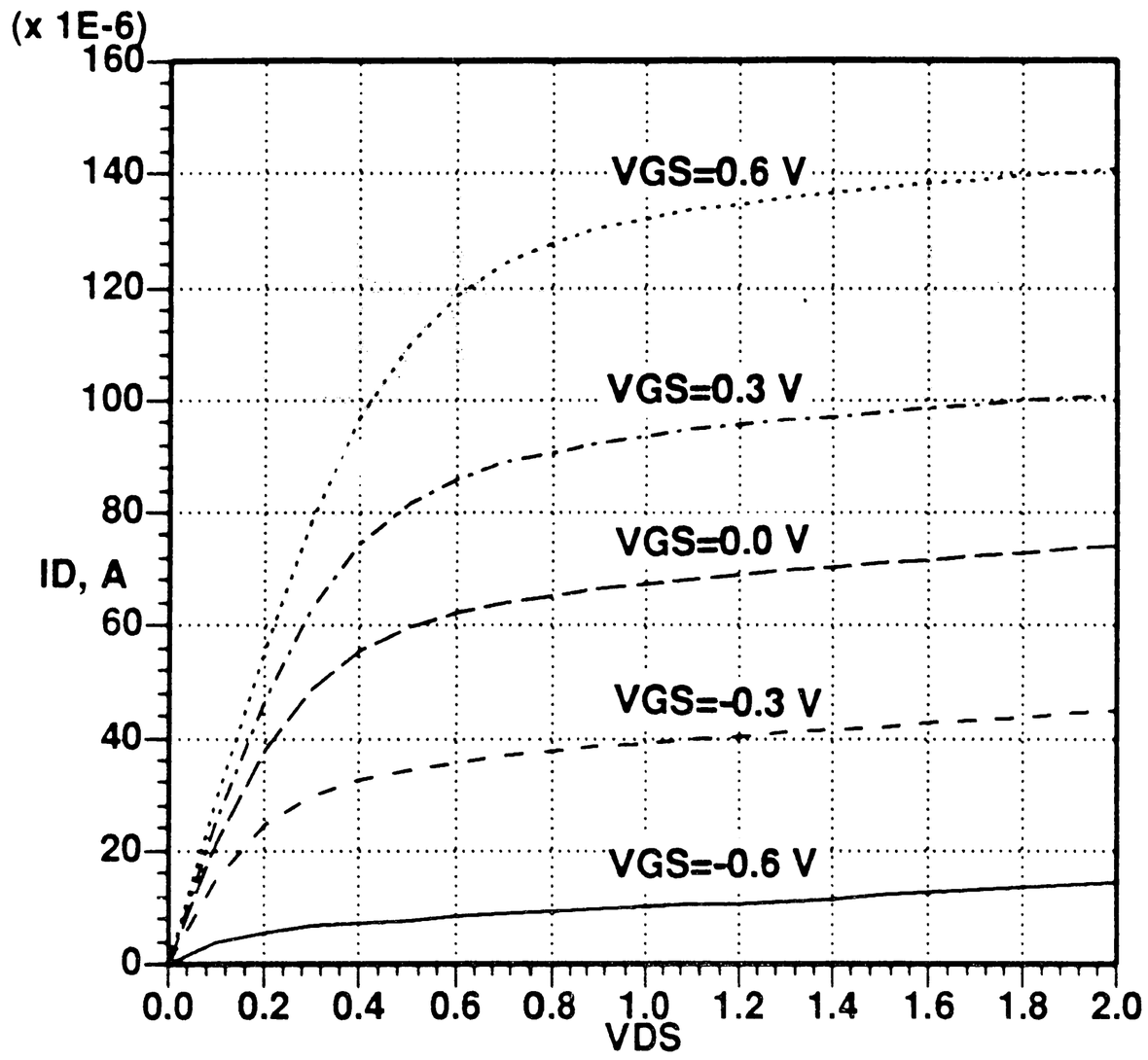


Figure 3.14. Nominal DFET IDS-VDS I/V characteristics at 125° C.

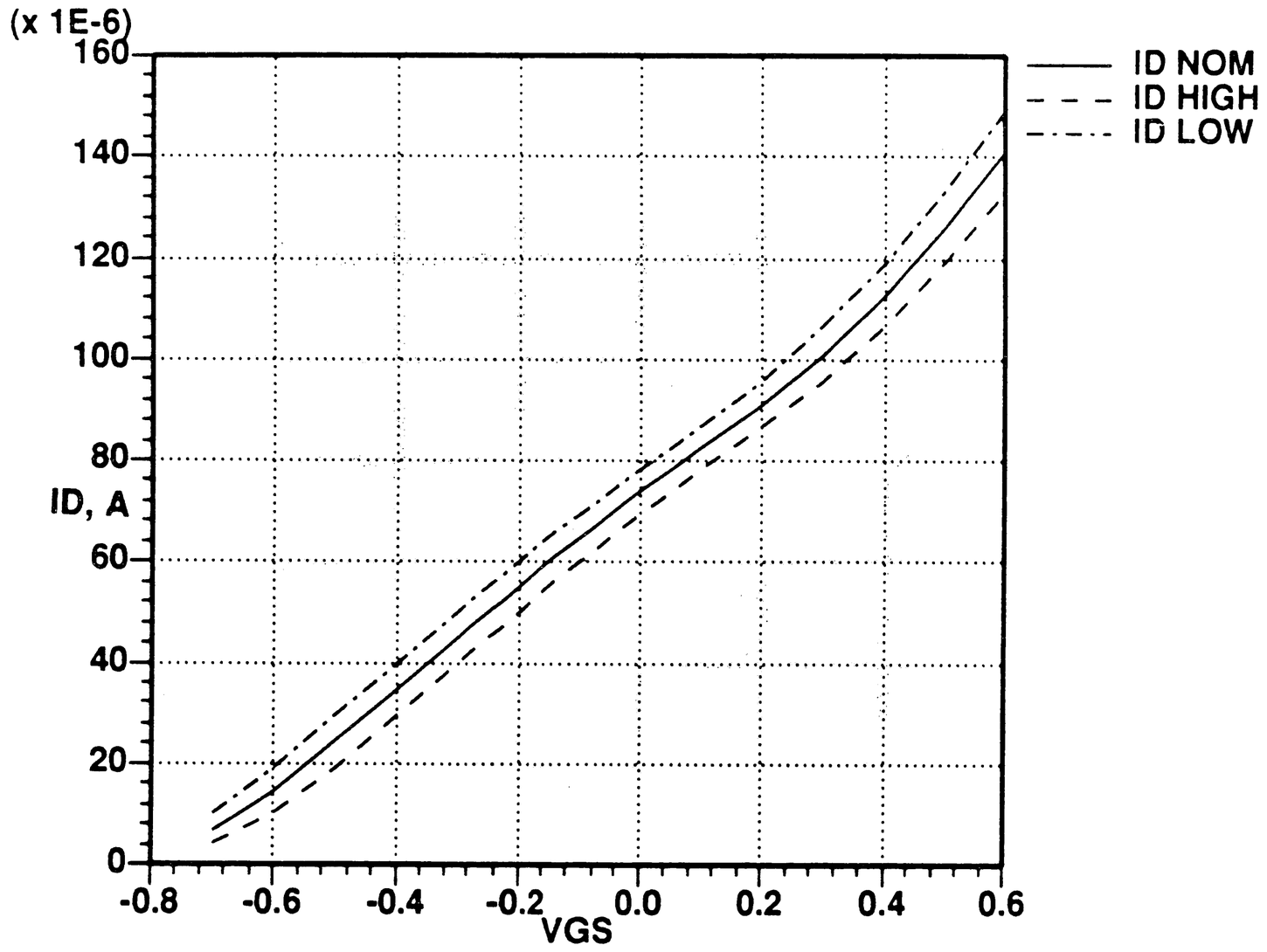


Figure 3.15. DFET IDS-VGS nominal, high, and low current characteristics at 125° C.

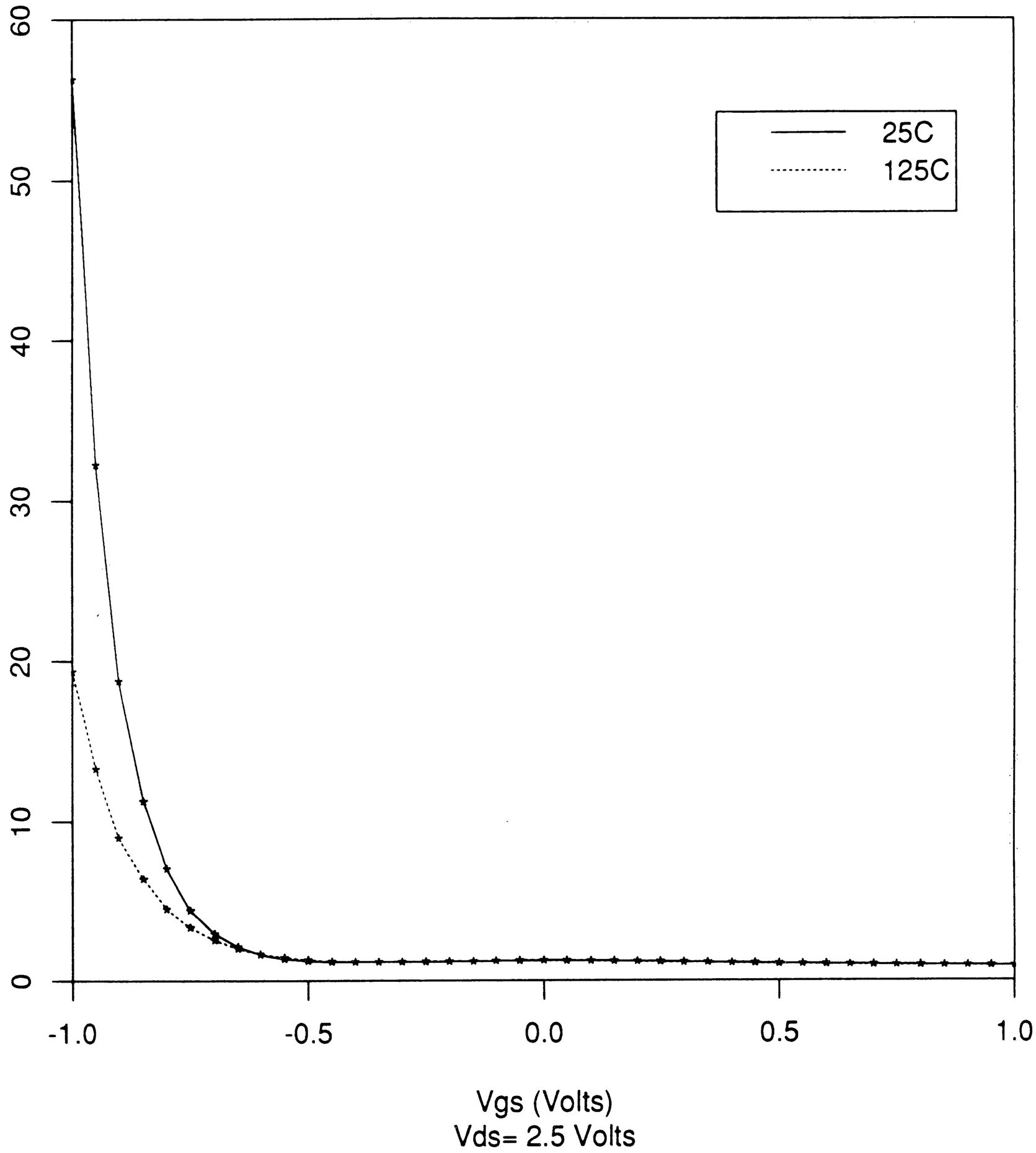


Figure 3.16. DFET gate and drain to source capacitances Cgs and Cgd at 25° and 125° C.

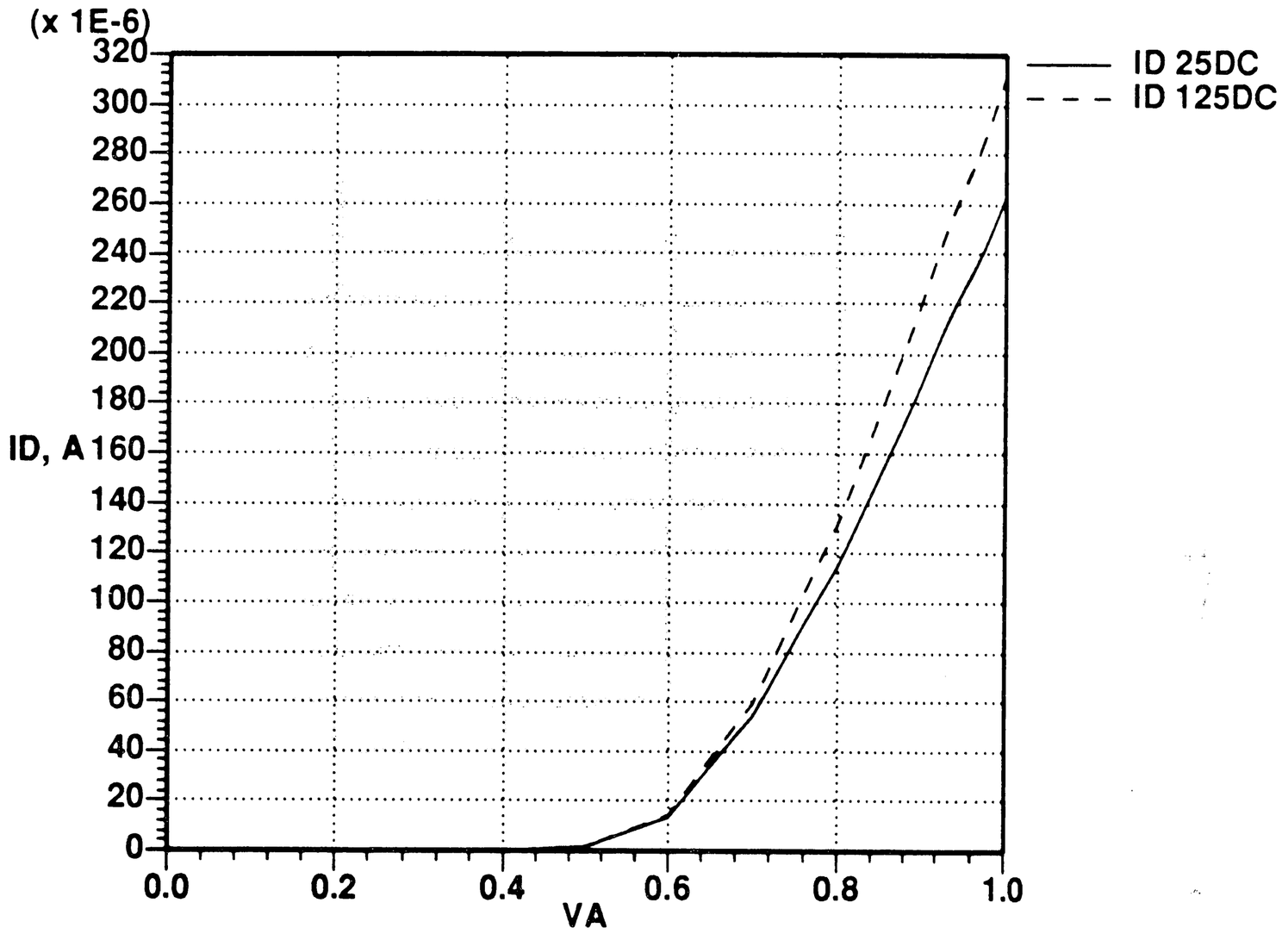


Figure 3.17. Schottky diode I/V characteristics at 25° C and 125° C.

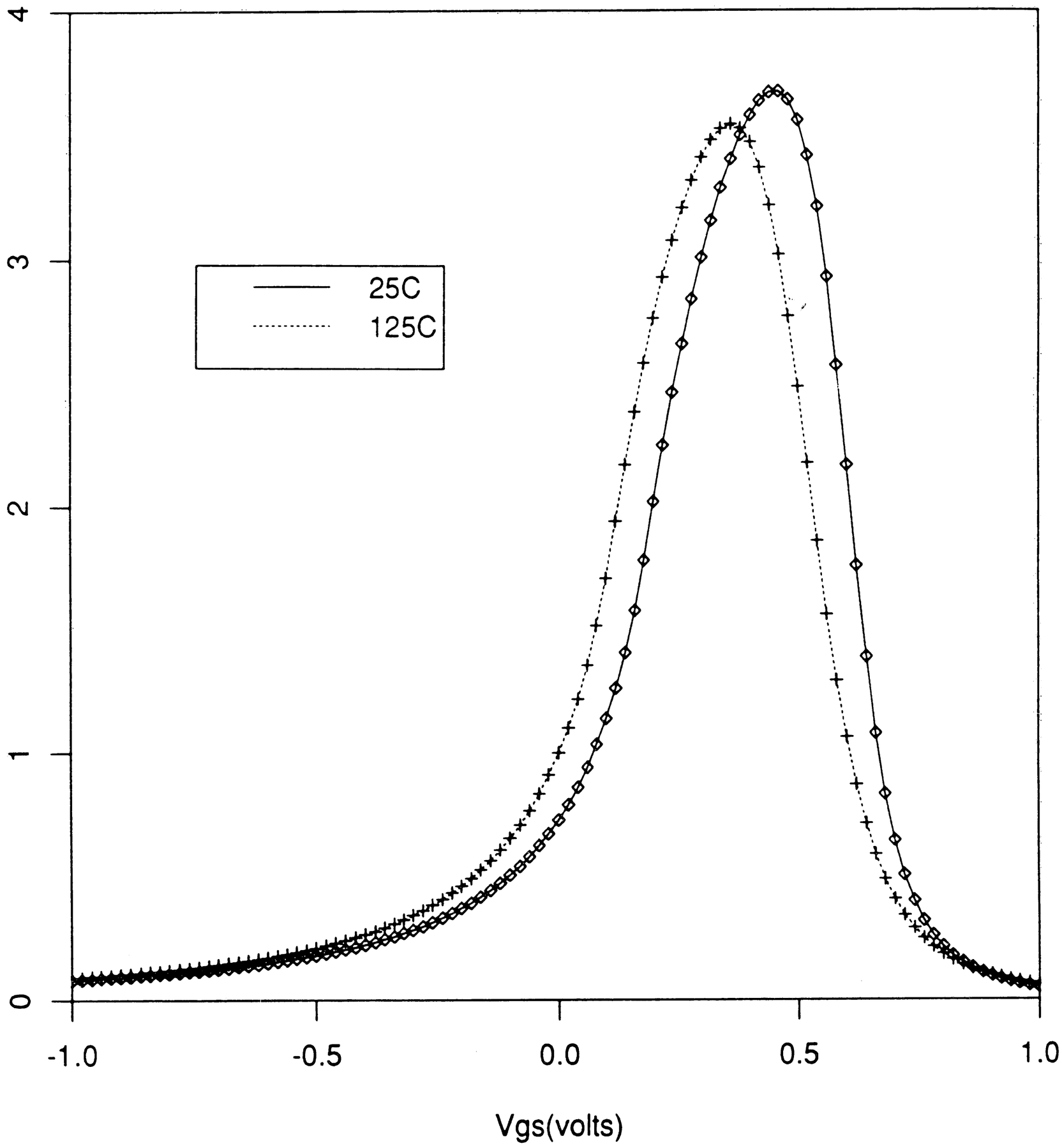


Figure 3.18. Schottky diode capacitance at 25° and 125° C.

CHAPTER 4

GaAs LOGIC FAMILY DESIGN

4.1. GaAs Logic Family Evolution

The feasibility of digital GaAs technologies was demonstrated using non-robust processes that only realized DFETs and Schottky diodes. The processes had poor threshold voltage control which required developing logic gates with large voltage swing and high noise margins. Hence, these families did not take advantage of GaAs's ability to operate at low power-supply voltages to reduce circuit power dissipation.

Buffered FET Logic (BFL) [12] was the first family developed. BFL is a high speed and high power logic family, that used an all DFET process and requires two power supplies. BFL has achieved loaded propagation delays of 33 pS at a power dissipation of 5-10 mW/gate. The high power dissipation of BFL limits the families' integration density to SSI and MSI.

Another logic family is the Source Coupled Logic (SCL) [13]. SCL is the FET version of bipolar Emitter-Coupled Logic (ECL) implemented with DFET technology, which uses a single power supply. The family has demonstrated 60 pS propagation delay at a power dissipation of 6 mW/gate. Due to its differential mode of operation SCL is very tolerant of threshold voltage variations, and operates over wide power supply voltages.

An improvement in the development of low power GaAs logic was the introduction of the Schottky Diode FET Logic (SDFL) [14]. SDFL is also based on an all DFET process, and like BFL it too required two power supplies. SDFL dissipates about one-fifth the power of BFL with a factor of two increase in propagation delay. The major attribute of SDFL is its low power that permits increases in circuit density to LSI levels [1]. However, the family is very fanout sensitive, since the gate is AC and DC loaded by fanout.

The advent of developing Enhancement mode devices realized the implementation of low power and high speed logic gates. The simplest logic family considered for an Enhancement/Depletion (E/D) technology was Direct Coupled FET Logic (DCFL) [15]. DCFL had the potential to achieve power dissipation as low as 50 μW/gate and propagation delay 2 to 4 times lower than BFL. The use of E/D FETs' allows DCFL to operate with a single power supply voltage as low as 1.0 V. DCFL has the potential to push GaAs integration density to VLSI levels due to its low power dissipation and simple design. However, the small voltage swing of DCFL (0.5 V) translates into small high and low DC noise margins of 200 mV or less at 300° K. The small noise margins place an overburdening constraint of achieving tight process parameter control.

The four logic families are shown in Figure 4.1, and Table 4.1 shows the salient features of these logic families.

TABLE 4.1

BFL, SCL, SDFL and DCFL LOGIC COMPARISON

BFL	SCL	SDFL	DCFL
HIGH SPEED/ HIGH FANOUT	HIGH SPEED/ HIGH FANOUT	MEDIUM SPEED/ LOW FANOUT	MEDIUM SPEED/ LOW FANOUT
HIGH POWER 5-10 mW/GATE	HIGH POWER 3-7 mW/GATE	MEDIUM POWER 2-5 mW/GATE	LOW POWER .1-.4 mW/GATE
GOOD DRIVER	GOOD DRIVER	POOR DRIVER	POOR DRIVER
LOW DENSITY	LOW DENSITY	MEDIUM DENSITY	HIGH DENSITY
2 POWER SUPPLIES	1 POWER SUPPLY	2 POWER SUPPLIES	1 POWER SUUPLY
NMH=0.5V NML=0.5V	NMH=0.5V NML=0.5V	NMH=0.4V NML=0.4V	NMH=200 mV NML=200 mV

4.2. Design and Analysis of LSI Grade GaAs Logic

A number of logic families that have the potential to realize LSI density in GaAs technology will be analyzed in this chapter. A back-of-the-envelope DC analysis is performed and compared with the simulated results for the families under consideration.

4.2.1 Direct Coupled FET Logic (DCFL) Analysis

A DCFL inverter is shown in Figure 4.2. DCFL is a simple logic family that has the potential for high density, speed, and low power dissipation. However, the analysis will show that the small DC noise margins of 200 mV at 300 K almost disappear at high temperatures. The family is not

robust to tolerate the wide process variations of present GaAs technology. DCFL logic has other problems, namely the inability to implement complex logic functions (AND/OR/INVERT) and its high fanout sensitivity due to Miller capacitance effect as will be shown in Chapter 5.

The output high level VOH of a loaded DCFL gate when the input is low is limited by the Schottky diode turn-on voltage of the load gate, which is 0.7 V. In order to simplify the analysis, an unloaded inverter is analyzed. The load device J1 in Figure 4.2 (a) is in saturation and driver J2 is in the linear region. The analysis uses the HFET I-V characteristics as derived by Shur [7]. The drain current in the linear region is given by Equation (4.1) and drain current and voltage in saturation are given by Equations (4.2) and (4.3) respectively.

$$I_{ds} = \beta \left[(V_{gs} - V_T) V_{ds} - \frac{1}{2} V_{ds}^2 \right] \qquad (4.1)$$

$$I_{ds} \approx \beta V_s^2 \left[\sqrt{1 + 2 \beta R_s (V_{gs} - V_T) + \frac{(V_{gs} - V_T)^2}{V_s^2}} - 1 \right] \qquad (4.2)$$

$$V_{ds} = (V_{gs} - V_T) + V_s - \sqrt{(V_{gs} - V_T)^2 + V_s^2} + I_{ds} (R_s + R_d) \qquad (4.3)$$

where:

$$\beta = \frac{\varepsilon \mu W}{(d + \Delta d) L_g} \qquad (4.4)$$

$$V_s = E_s L_g \qquad (4.5)$$

R_s and R_d are the source and drain resistances; ε is the permitivity of GaAs (12.9 E_0) μ is the mobility of 2 DEG (4500 cm^2/V s), Lg is the gate length, W is the width, E_S is the velocity saturated electric field, and d+ Δd is the distance to the 2 DEG. For an EFET d+ Δd =600 Å and for a DFET d+ Δd = 1000 Å. The voltage V_S is the voltage at which velocity saturation occurs and it is about 0.3 V. The EFET threshold voltage is 250 mV and DFET threshold is -600 mV.

The DCFL inverter will be analyzed to get the transfer characteristics as shown in Figure 4.3. This analysis will then be used as the basic building block for analyzing the other logic families discussed.

CASE 1: $V_{IN} = V_{OH}$

The drain current of J1 is given by equation (4.6), and J2's current is given by Equation (4.7). Equating the two currents we get:

$$I_{d1} = \beta_D V_s^2 \left[\sqrt{\left[1 - 2\beta_D R_{sD} V_{TD} + \frac{V_{TD}^2}{V_s^2} \right]} - 1 \right] \qquad (4.6)$$

$$I_{d2} = \beta_E \left[(V_{IN} - V_{TE})\, Vo - \frac{1}{2} Vo^2 \right] \qquad (4.7)$$

Rearranging terms we find that:

$$\beta_E Vo^2 - 2\beta_E (V_{IN} - V_{TE})\, Vo + 2\beta_D V_s^2 \left[\sqrt{\left[1 - 2\beta_D R_{sD} V_{TD} + \frac{V_{TD}^2}{V_s^2} \right]} - 1 \right] = 0 \qquad (4.8)$$

using the quadratic formula and taking the negative root:

$$Vo = \frac{2\beta_E(V_{IN} - V_{TE}) - \sqrt{\left[(2\beta_E(V_{IN} - V_{TE}))^2 - 8\beta_E\beta_D V_s^2\left(\sqrt{\left(1 - 2\beta_D R_{sD} V_{TD} + \frac{V_{TD}^2}{V_s^2}\right)} - 1\right)\right]}}{2\beta_E} \qquad (4.9)$$

Using the device sizes from Figure 4.2 with a gate length of 1 μm. The EFET source resistance of 200 Ω, and DFET source resistance of 625 Ω. The output Vo is: $Vo = V_{OL} = 0.14$ V.

CASE 2: $V_{IN} < V_{TE}$

When the input is less than or equal to V_{TE} of the driver J2, then the output will equal V_{OH} which is VDD: $Vo = V_{OH} = VDD = 2.0$ V

CASE 3: $V_{IN} = V_{IL}$

In this case we will assume that J1 will be in the linear region and J2 is in saturation, hence the drain currents and the output VO are written as:

$$I_{d1} = \beta_D\left[-V_{TD}(VDD - Vo) - \frac{1}{2}(VDD - Vo)^2\right] \approx \beta_D\,[-V_{TD}(VDD - Vo)] \qquad (4.10)$$

since the output VOH will be very close to VDD, the term $(VDD - VO)^2$ can be neglected to yield:

$$I_{d1} = \beta_D V_{TD} Vo - \beta_D V_{TD} VDD \qquad (4.11)$$

$$I_{d2} = \beta_E V_s^2 \left[\sqrt{\left[1 + 2\beta_E R_{sE}(V_{IN} - V_{TE}) + \frac{(V_{IN} - V_{TE})^2}{V_s^2} \right]} - 1 \right] \qquad (4.12)$$

$$Vo = (V_{IN} - V_{TE}) + V_s - [(V_{IN} - V_{TE})^2 + V_s^2]^{\frac{1}{2}} + 2R_{sE}I_{d2} \qquad (4.13)$$

the V_{IL} level for DCFL will be near V_{TE}, thus the term $(V_{IN} - V_{TE})^2$ is much less than V_s^2 and can be neglected:

$$Vo = (V_{IN} - V_{TE}) + 2R_{sE}I_{d1} \ , \ I_{d1} = I_{d2} \qquad (4.14)$$

$$Vo = V_{IN} - V_{TE} + 2R_{sE}\beta_D V_{TD} Vo - 2R_{sE}\beta_D V_{TD} VDD \qquad (4.15)$$

solving for Vo :

$$Vo = \frac{V_{IN} - V_{TE} - 2\beta_D R_{sE} V_{TD} VDD}{1 - 2\beta_D R_{sE} V_{TD}} \qquad (4.16)$$

to find the unity gain point at which $V_{IN} = V_{IL}$, the derivative of VO with respect to V_{IN} is set equal to -1.

$$\frac{dVo}{dV_{IN}} = \frac{dVo}{dI_{d1}} \frac{dI_{d1}}{dV_{IN}} = \frac{dVo}{dI_{d1}} \frac{dI_{d2}}{dV_{IN}} = -1 \qquad (4.17)$$

$$\frac{dVo}{dI_{d1}} = \frac{1}{\beta_D V_{TD}} \qquad (4.18)$$

since $\frac{(V_{IN} - V_{TE})^2}{V_s^2} << 2\beta_E R_{sE} (V_{IN} - V_{TE})$, Id2 can be written as:

$$I_{d2} = \beta_E V_s^2 \sqrt{[\,1 + 2\beta_E R_{sE}\,(V_{IN} - V_{TE})]} - \beta_E V_s^2 \qquad (4.19)$$

$$\frac{dI_{d2}}{dV_{IN}} = \frac{\beta_E V_s^2 R_{sE}}{\sqrt{[\,1 + 2\beta_E R_{sE}\,(V_{IN} - V_{TE})]}} \qquad (4.20)$$

$$\frac{dVo}{dI_{d1}}\,\frac{dI_{d2}}{dV_{IN}} = \frac{\beta_E^2 V_s^2 R_{sE}}{\beta_D V_{TD}\sqrt{[\,1 + 2\beta_E R_{sE}\,(V_{IN} - V_{TE})]}} = -1 \qquad (4.21)$$

solving for $V_{IN} = V_{IL}$:

$$V_{IN} = \frac{\beta_E^4 V_s^4 R_{sE}^2 + 2\beta_E \beta_D^2 V_{TD}^2 R_{sE} V_{TE} - \beta_D^2 V_{TD}^2}{2\beta_E \beta_D^2 V_{TD}^2 R_{sE}} \qquad (4.22)$$

from which we get a value for $V_{IN} = V_{IL} = 0.290$ V. The output voltage VO can be written as :

$$Vo = \frac{I_{d1} + \beta_D V_{TD} VDD}{\beta_D V_{TD}}\,, \quad I_{d1} \approx 64\,\mu A \qquad (4.23)$$

$$Vo = 1.9 \text{ V}$$

At a V_{IL} value of 0.29 V and Vo value of 1.9 V, J1 will be in the linear region and J2 in saturation as assumed.

CASE 4: $V_{IN} = V_{IH}$

For this case it is assumed that J1 in saturation and J2 in linear regions, hence:

$$I_{d1} = \beta_D V_s^2 \left[\sqrt{\left[1 - 2\beta_D R_{sD} V_{TD} + \frac{V_{TD}^2}{V_s^2} \right]} - 1 \right] \qquad (4.24)$$

$$I_{d2} = \beta_E \left[(V_{IN} - V_{TE})\, Vo - \frac{1}{2} Vo^2 \right] \qquad (4.25)$$

equating terms and solving for VO and V_{IN} respectively:

$$\beta_E Vo^2 - 2\beta_E Vo V_{IN} + 2\beta_E V_{TE} Vo + 2\beta_D V_s^2 \left[\sqrt{\left[1 - 2\beta_D R_{sD} V_{TD} + \frac{V_{TD}^2}{V_s^2} \right]} - 1 \right] \qquad (4.26)$$

$$V_{IN} = \frac{1}{2} Vo + V_{TE} + \frac{\beta_D V_s^2}{\beta_E} \left[\sqrt{\left[1 - 2\beta_D R_{sD} V_{TD} + \frac{V_{TD}^2}{V_s^2} \right]} - 1 \right] Vo^{-1} \qquad (4.27)$$

The derivative of V_{IN} with respect to VO is set equal to -1 to solve for VO:

$$\frac{dV_{IN}}{dVo} = \frac{1}{2} - \frac{\beta_D V_s^2}{\beta_E} \left[\sqrt{\left[1 - 2\beta_D R_{sD} V_{TD} + \frac{V_{TD}^2}{V_s^2} \right]} - 1 \right] Vo^{-2} = -1 \qquad (4.28)$$

$$Vo = \left[\frac{2}{3} \frac{\beta_D V_s^2}{\beta_E} \left[\sqrt{\left[1 - 2\beta_D R_{sD} V_{TD} + \frac{V_{TD}^2}{V_s^2} \right]} - 1 \right] \right]^{\frac{1}{2}} \qquad (4.29)$$

Vo = 0.15 V.

Thus J1 will be saturated and J2 in linear region. Solving for V_{IH} we get:

$$V_{IH} = \frac{1}{2} Vo + V_{TE} + \frac{\beta_D V_s^2}{\beta_E} \left[\sqrt{\left[1 - 2\beta_D R_{sD} V_{TD} + \frac{V_{TD}^2}{V_s^2} \right]} - 1 \right] Vo^{-1} \qquad (4.30)$$

$$V_{IH} = 0.55 \text{ V}.$$

The calculated and simulated transfer characteristics for the DCFL inverter are shown in Figure 4.3. The simulated transfer curve shows the output voltage increasing as the input exceeds 0.7 V. This effect is observed due to conduction by the Schottky diode of J2 at forward bias. Hence, the loaded output voltage high of a DCFL inverter will be clamped near 0.7 V, and reduces the inverter's Noise Margin High.

The loaded transfer characteristics for the DCFL gate are shown in Chapter 5, from which the DC noise margins are extracted.

Figure 4.3 shows that DCFL has a very poor Noise Margin Low, thus series connection of EFETs to make NAND gates or complex gates is not feasible. Hence, DCFL logic must be synthesized with NOR gates. A schematic of a NOR gate SR latch and its transient response are shown in Figures 4.4 and 4.5. A clocked latch implemented in DCFL with its simulated transient response is also shown in Figures 4.6 and 4.7.

4.2.2. Source Follower Logic (SFL) Analysis

The noise margins of a DCFL gate can be improved by using a source follower stage to drive a DCFL inverter as shown in Figure 4.8 (a). The analysis of the SFL logic family will proceed by finding the transfer characteristics of the source follower input. The SFL inverter will be characterized as a source follower driving a DCFL inverter, hence the V_{IL}, V_{IH}, V_{OL}, and V_{OH} values from the DCFL analysis will be used. Since the voltage swing at node VO1 is clamped by the Schottky diode of the DCFL driver EFET, DFET J2 will be in the linear region and J1 is saturated. The analysis will be simplified by neglecting the Schottky diode current of the DCFL inverter.

$$I_{d1} = \beta_{E1} V_s^2 \left[\sqrt{\left[1 = 2\beta_{E1} R_{sE1} (V_{IN} - V_{TE} - Vo1) + \frac{(V_{IN} - V_{TE} - Vo1)^2}{v_s^2} \right]} - 1 \right] \qquad (4.31)$$

$$I_{d2} = \beta_{D1} \left[-V_{TD} Vo1 - \frac{1}{2} Vo1^2 \right] \qquad (4.32)$$

$$(I_{d2})^2 = \beta_{D1}^2 \left[V_{TD}^2 Vo1^2 + \frac{1}{4} Vo1^4 + V_{TD} Vo1^3 \right] \approx \beta_{D1}^2 [V_{TD}^2 Vo1^2 + V_{TD} Vo1^3] \qquad (4.33)$$

since the term $(1/4)\beta_{D1}V_{01}^4$ is smaller than the cube and square terms. Squaring I_{d1} and neglecting the term $\beta_{E1}^2 Vs^2$,

since it is very small:

$$(I_{d1})^2 = \beta_{E1}^2 V_s^2 [V_{IN}^2 + Vo1^2 + V_{TE}^2 + 2V_{TE}Vo1 - 2V_{IN}Vo1 - 2V_{IN}V_{TE}] + 2\beta_{E1}^3 V_s^2 R_{sE1}(V_{IN} - V_{TE} - Vo1) \quad (4.34)$$

equating $(I_{d1})^2 = (I_{d2})^2$:

$$\beta_{D1}^2 V_{TD} Vo1^3 + \beta_{D1}^2 V_{TD}^2 Vo1^2 - \beta_{E1}^2 V_s^2 Vo1^2 - 2\beta_{E1}^2 V_s^2 (V_{TE} - V_{IN})\, Vo1 + 2\beta_{E1}^3 V_s^2 R_{sE1} Vo1 - \beta_{E1}^2 V_s^2 (V_{IN}^2 + V_{TE}^2 - 2V_{IN}V_{TE}) - 2\beta_{E1}^3 V_s^2 R_{sE1} (V_{IN} - V_{TE}) = 0 \quad (4.35)$$

since V_{O1} is clamped to about 0.7 V, the cube term will be much smaller then the square term for V_{O1}. Solving for V_{O1} using the quadratic formula and taking the positive root:

$$Vo1 = \frac{-b + \sqrt{[b^2 - 4ac]}}{2a} \quad (4.36)$$

where

$$a = \beta_{D1}^2 V_{TD}^2 - \beta_{E1}^2 V_s^2 \quad (4.37)$$

$$b = -2\beta_{E1}^2 V_s^2 (V_{TE} - V_{IN}) + 2\beta_{E1}^3 V_s^2 R_{sE1} \quad (4.38)$$

$$c = \beta_{E1}^2 V_s^2 (V_{IN}^2 + V_{TE}^2 - 2V_{IN}V_{TE}) + 2\beta_{E1}^3 V_s^2 R_{sE1} (V_{IN} - V_{TE}) \quad (4.39)$$

The source follower transfer characteristics are plotted in Figure 4.9 assuming that V_{O1} will be clamped by the EFET Schottky diode. Using the the DCFL data for V_{IL}, V_{IH}, V_{OL}, and V_{OH}, those points can be calculated for the SFL inverter. The simulated and calculated SFL transfer characteristics are shown in Figure 10.

$V_{IN} = V_{OH}$: V_{O1} = 0.7 V and V_{OL} = 0.14 V
$V_{IN} = V_{IL}$: V_{O1} = 0.29 V and V_{IL} = 0.6 V, VO = 1.9 V
$V_{IN} = V_{IH}$: V_{O1} = 0.55 V and V_{IH} = 0.95 V, VO = 0.15 V
$V_{IN} = V_{OL}$: V_{O1} = 0 and V_{OH} = VDD = 2.0 V

By looking at the 2 input NOR gate in Figure 4.8 (b), we see when both inputs are high, the Schottky diode of J5 in the output stage can conduct excessive current supplied through J2 and J3. The excess current can be limited by adding a DFET to the gate as shown in Figure 4.11. This addition to the gate does not affect the transfer characteristics of the gate as shown in Figure 4.12, and helps reduce the gate's power dissipation.

It can be seen that SFL has higher noise margins than DCFL and makes a more robust logic family tolerant of process and temperature variations. Furthermore, the higher Noise Margin Low of SFL allows the series connection of EFETs in the output stage to implement NAND gates and complex gates such as OR/AND/INVERT shown in Figure 4.13 with a single gate delay.

The SFL gate can be used to built OR/AND/INVERT gates with a single gate delay as shown in Figure 4.13. Also SR and clocked latches (see Figures 4.14 thru 4.17) can be built with only two gate delays.

4.2.3. Push/Pull Source Follower Logic Analysis

One drawback of both DCFL and SFL logic is the ratioed E/D output stage. The output stage is inefficient for driving large capacitive loads, and dissipates a lot of DC power when the output is low. An improvement for SFL is to replace the E/D output stage by a driven all EFET push/pull stage as shown in Figure 4.18.

When the input to the SFL gate in Figure 4.18 is high, then node C is at approximately 1.2 V, node D is at about 0.7 V, and the output will be low. Since j5 acts as a diode when the output is low, then the gate to source voltage of j4 is about 0.3 V. Hence, the DC power will be minimized in the low state. When the input goes low node C switches faster than the output Z, and j5 develops a large gate to source voltage which dumps a large current to charge the load capacitance. In the push/pull stage j5 acts as a level shifter. The DC transfer curve for this gate is shown in Figure 4.19. The SFL gate analysis can be applied to the push/pull SFL and will yield similar analytical results.

The push/pull type of SFL also has a high Noise Margin Low and can be used to built NAND and OR/AND/INVERT gates with a single gate delay. The family can also be used to built SR and clocked latches with only two gate delays as shown in Figures 4.20 thru 4.24.

As can be seen SFL has much higher DC noise margins than DCFL, but the gate uses more layout area and dissipates more

power. However, the ability to implement complex gates in SFL can overcome such penalties. Another major advantage of SFL is the lower fanout sensitivity of the source follower input stage as will be shown in Chapter 5.

4.2.4 FET Injection Logic (FIL) Analysis

A FET Injection Logic (FIL) inverter is shown in Figure 4.25. This family is a current steering logic similar to IIL gate. The basic gate in FIL is the NAND function. The inputs to an FIL gate are wire ANDed and the outputs are multiple open drains. The family operates as follows:

The input is driven by open drain output. When the input is low, current Id1 is sunk into the driver and outputs J3 and J4 are high (OFF). If the input is high, then Id1 is driven into J2 and node C turns J3 and J4 on and the outputs go low. Diode D1 acts as a level shifter, while D2 acts as a speed up capacitor.

The analysis of the FIL inverter is carried out by finding the gate to source voltage VOD of J2 as shown in Figure 4.26. Then the DCFL analysis will be used to predict the transfer characteristics of the FIL inverter. When the input current Iin is zero, J1 will be in the linear region and J2 is off. The maximum value of VOD is limited by the gate/source Schottky diode of J2, hence, J1 will be in the linear region of operation.

$$I_{d1} = -\beta_D \left(V_{TD}\, VOD + \frac{1}{2} VOD^2 \right) \qquad (4.40)$$

$$I_{d1} = \beta_D \left(-V_{TD}\, VOD - \frac{1}{2} VOD^2 \right) \qquad (4.41)$$

$$VOD = f(I_{in}) \qquad (4.42)$$

equating (4.40) and (4.41) and rearranging terms, we get:

$$\beta_D VOD^2 + 2\beta_D V_{TD} VOD + 2I_{IN} = 0 \qquad (4.43)$$

solving for the voltage VOD and taking the negative root:

$$VOD = \frac{-2\beta_D V_{TD} - \sqrt{[4\beta_D^2 V_{TD}^2 - 8\beta_D I_{IN}]}}{2\beta_D} \qquad (4.44)$$

By substituting the DCFL V_{IL}, V_{IH}, V_{OL}, and V_{OH} values, the transfer characteristic of the FIL inverter can be derived. From the DCFL transfer analysis, the input current low and high values can be calculated. The output voltage low and high will be the same as the DCFL inverter.

$I_{IN} = I_{OH}$: VOD = 0.7 V and V_{OL} = 0.14 V
$I_{IN} = I_{IL}$: VOD = 0.29 V and I_{IL} = 200 uA
$I_{IN} = I_{IH}$: VOD = 0.55 V and I_{IH} = 275 uA
$I_{IN} = I_{OL}$: VOD = 0 and V_{OH} = VDD = 2.0 V

Figure 4.27 shows the calculated and simulated DC transfer characteristics of the unloaded FIL inverter as a function of the input current I_{IN}.

The transfer characteristics for the FIL logic family show that it is robust and has high DC noise margins in the

low and high states. The noise margins and characteristics will be discussed further in Chapter 5.

The FIL family implements the NAND function by having wired inputs and multiple open drain outputs as shown in Figure 4.28 for a 2 input NAND gate with two outputs. A NOR gate can also be implemented in FIL as shown in Figure 4.29. The open drain outputs will be pulled up by the input of the driven stage.

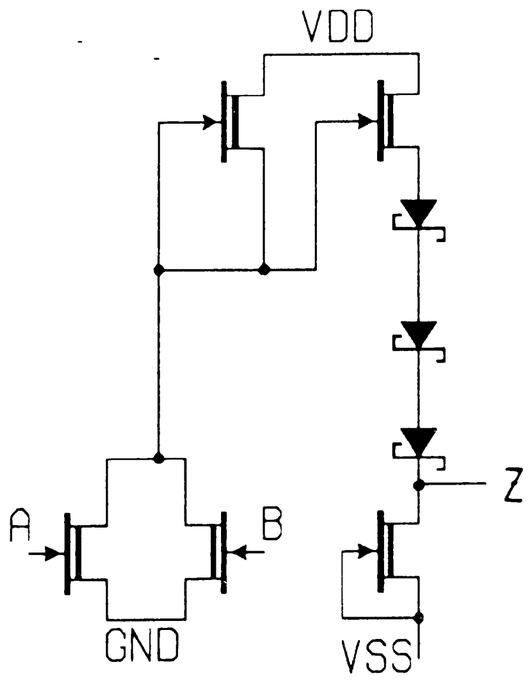
FIL can implement complex gates such as AND/OR/INVERT logic with a single gate delay as shown in Figure 4.30. The family can also implement NAND SR latches, as well as clocked complex latches as shown in Figures 4.31 thru 4.34.

Table 4.2 compares the salient characteristics of DCFL, SFL, and FIL logic families. All logic families are operated from a single 2.0 V power supply.

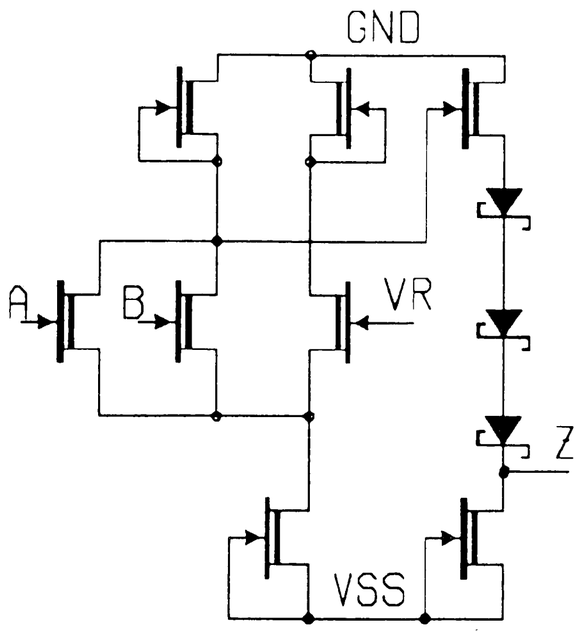
TABLE 4.2

DCFL, SFL, and FIL LOGIC COMPARISON

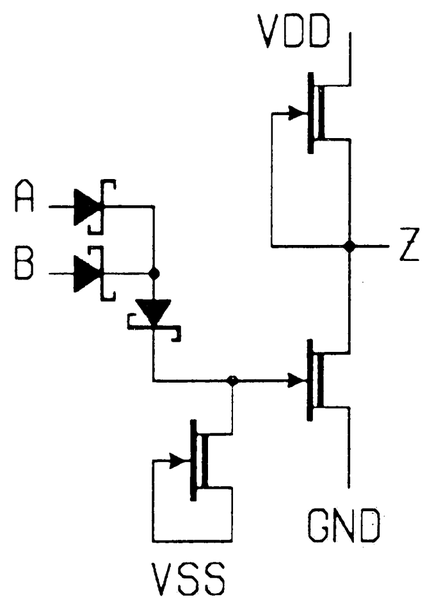
DCFL	SFL	PUSH/PULL SFL	FIL
MEDIUM SPEED/ LOW FANOUT	MEDIUM SPEED/ HIGH FANOUT	HIGH SPEED/ HIGH FANOUT	MEDIUM SPEED/ LOW FANOUT
LOW POWER .1-.4 mW/GATE	MEDIUM POWER .5-.9 mW/GATE	MEDIUM POWER .3-.6 mW/GATE	LOW POWER .2-.5 mW/GATE
POOR DRIVER	GOOD DRIVER	GOOD DRIVER	POOR DRIVER
HIGH DENSITY	HIGH DENSITY	HIGH DENSITY	HIGH DENSITY
NMH=0.15 V NML=0.2 V	NMH=0.5 V NML=0.5 V	NMH=0.3 V NML=0.4 V	NMH=0.3 V NML=0.6 V
NO COMPLEX GATES	COMPLEX GATES	COMPLEX GATES	COMPLEX GATES



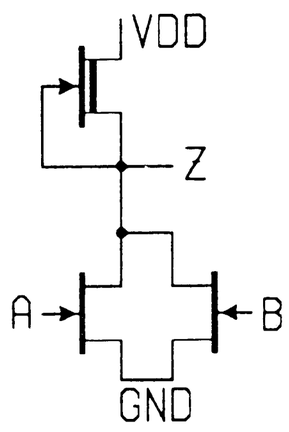
(a)



(b)

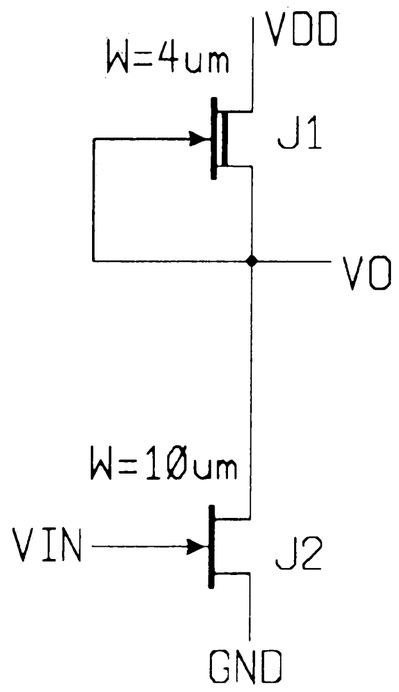


(c)

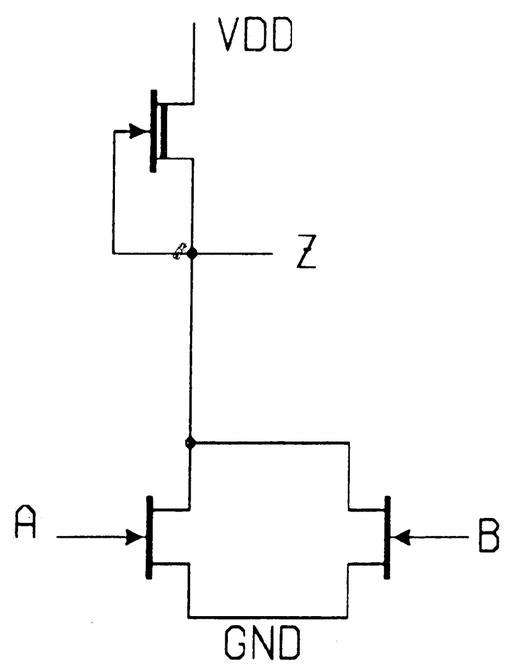


(d)

Figure 4.1. (a) BFL 2 input NOR gate, (b) SCL 2 input NOR gate, (c) SDFL 2 input NOR gate, (d) DCFL 2 input NOR gate.



(a)



(b)

Figure 4.2. (a) DCFL Inverter (b) DCFL 2 input NOR gate.

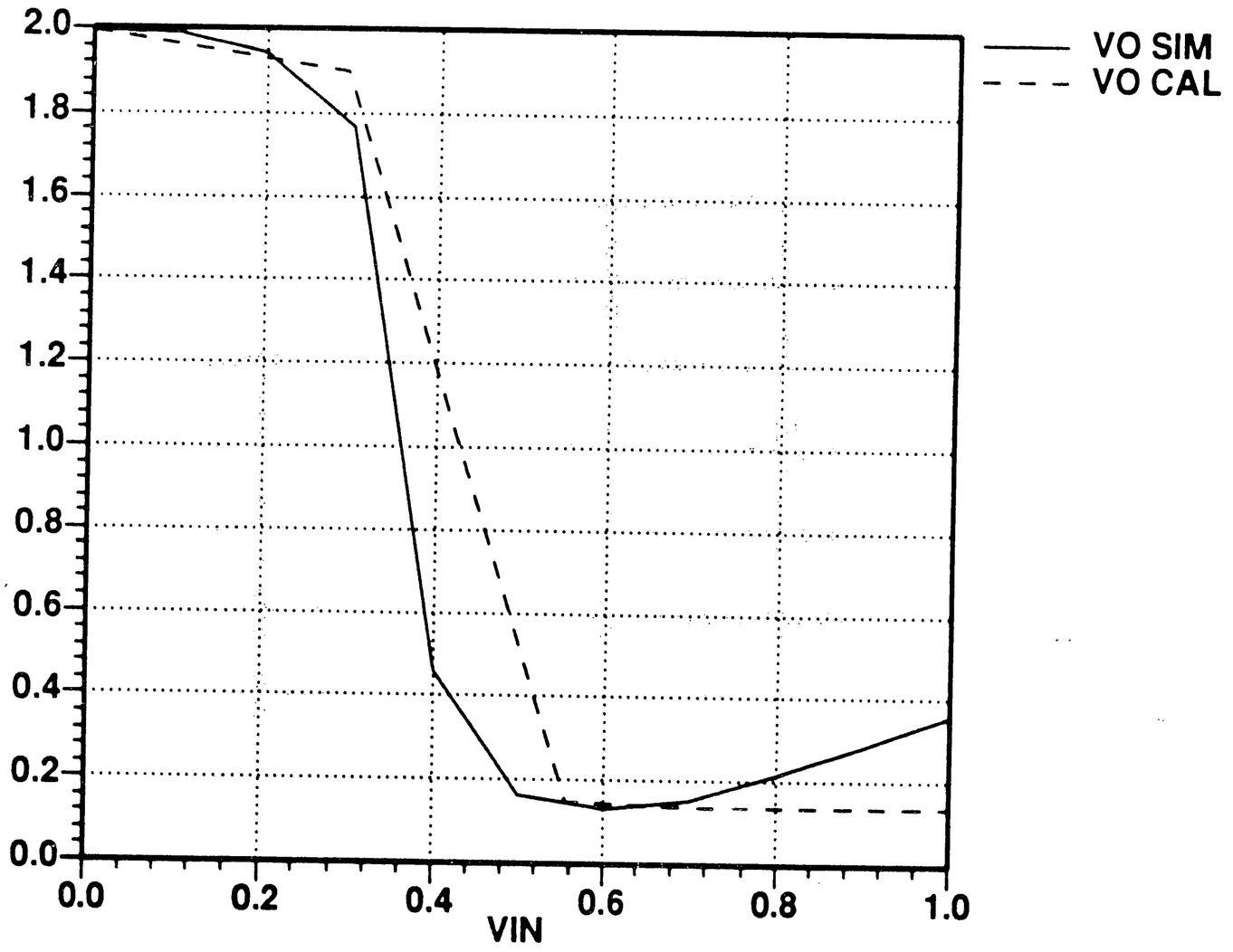


Figure 4.3. Calculated and simulated unloaded DCFL transfer curve.

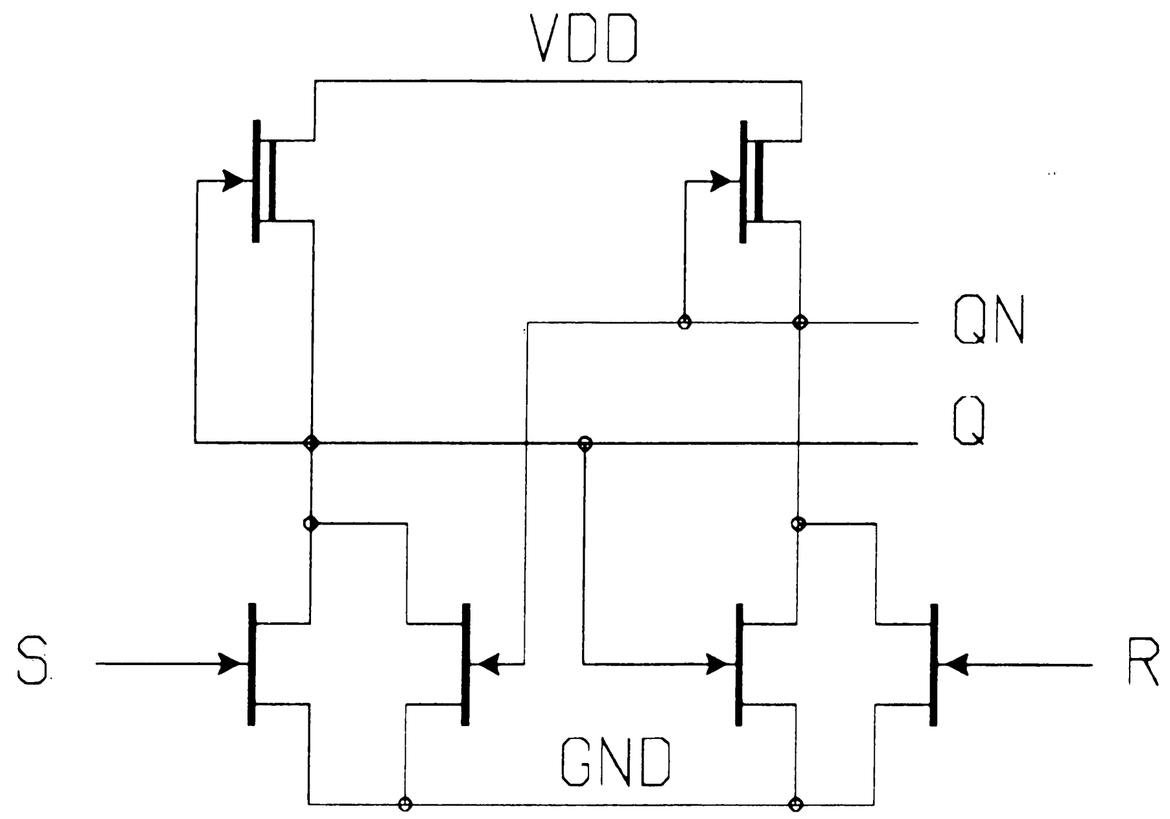


Figure 4.4. SR DCFL latch.

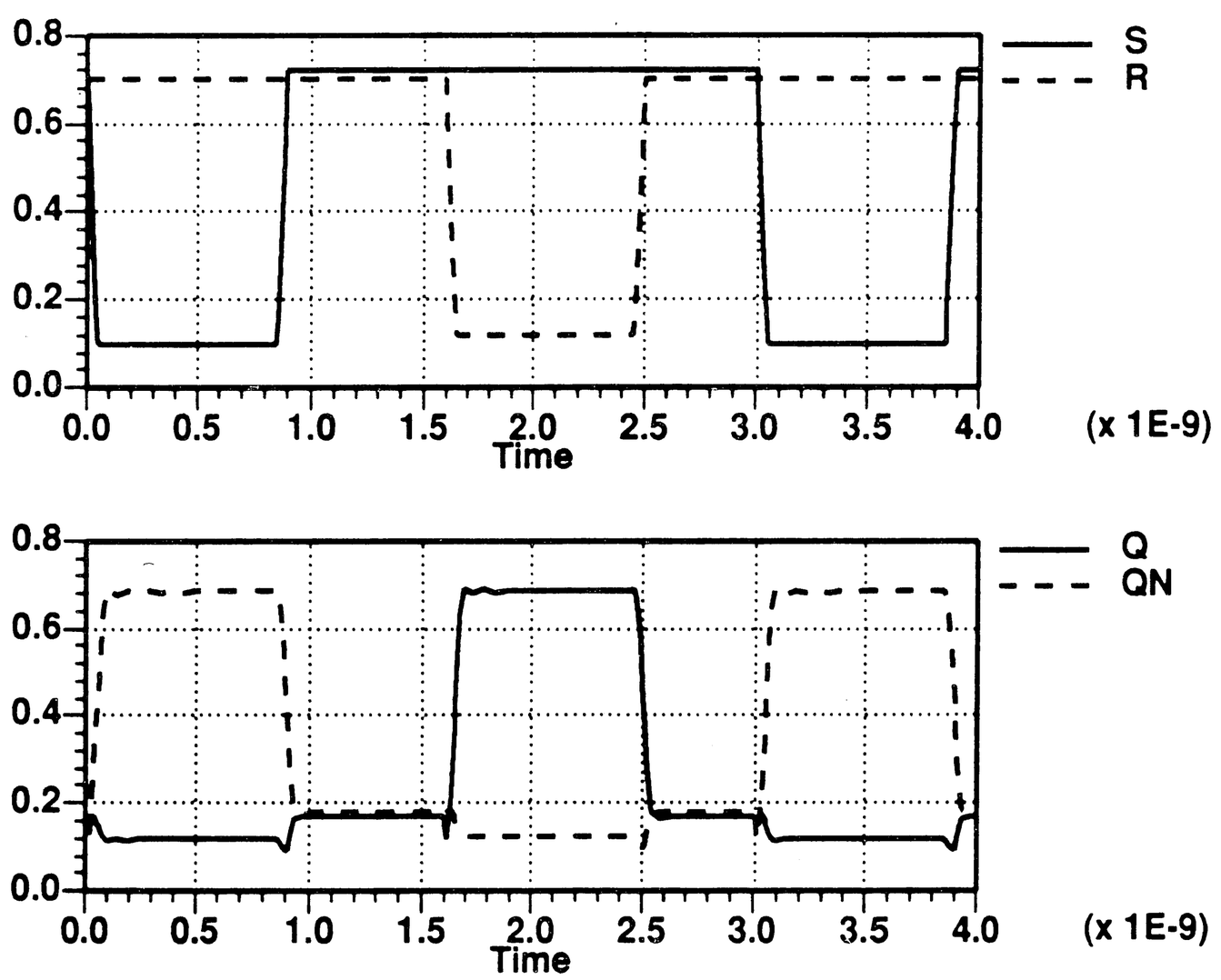


Figure 4.5. DCFL SR latch response.

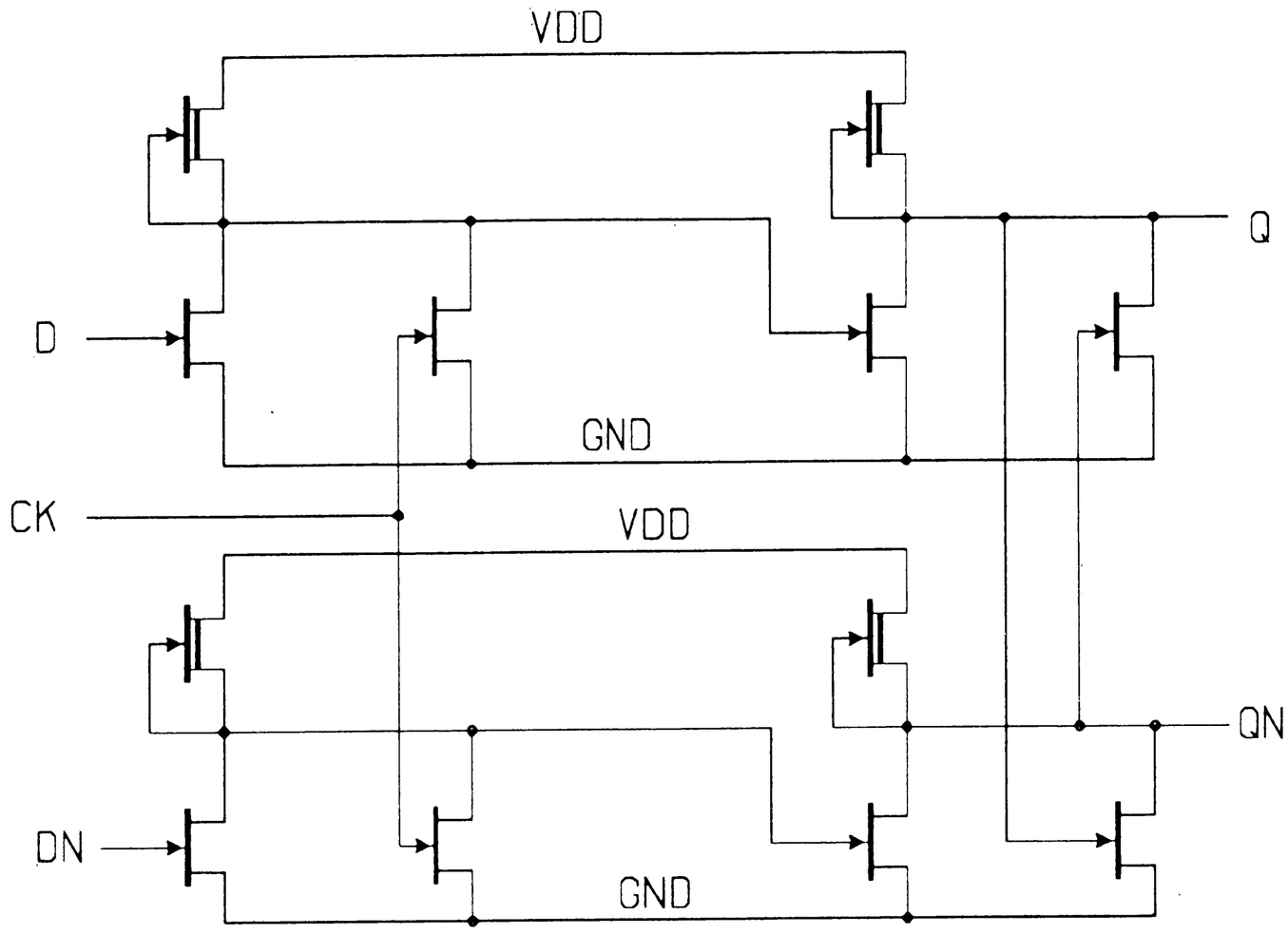


Figure 4.6. DCFL clocked latch.

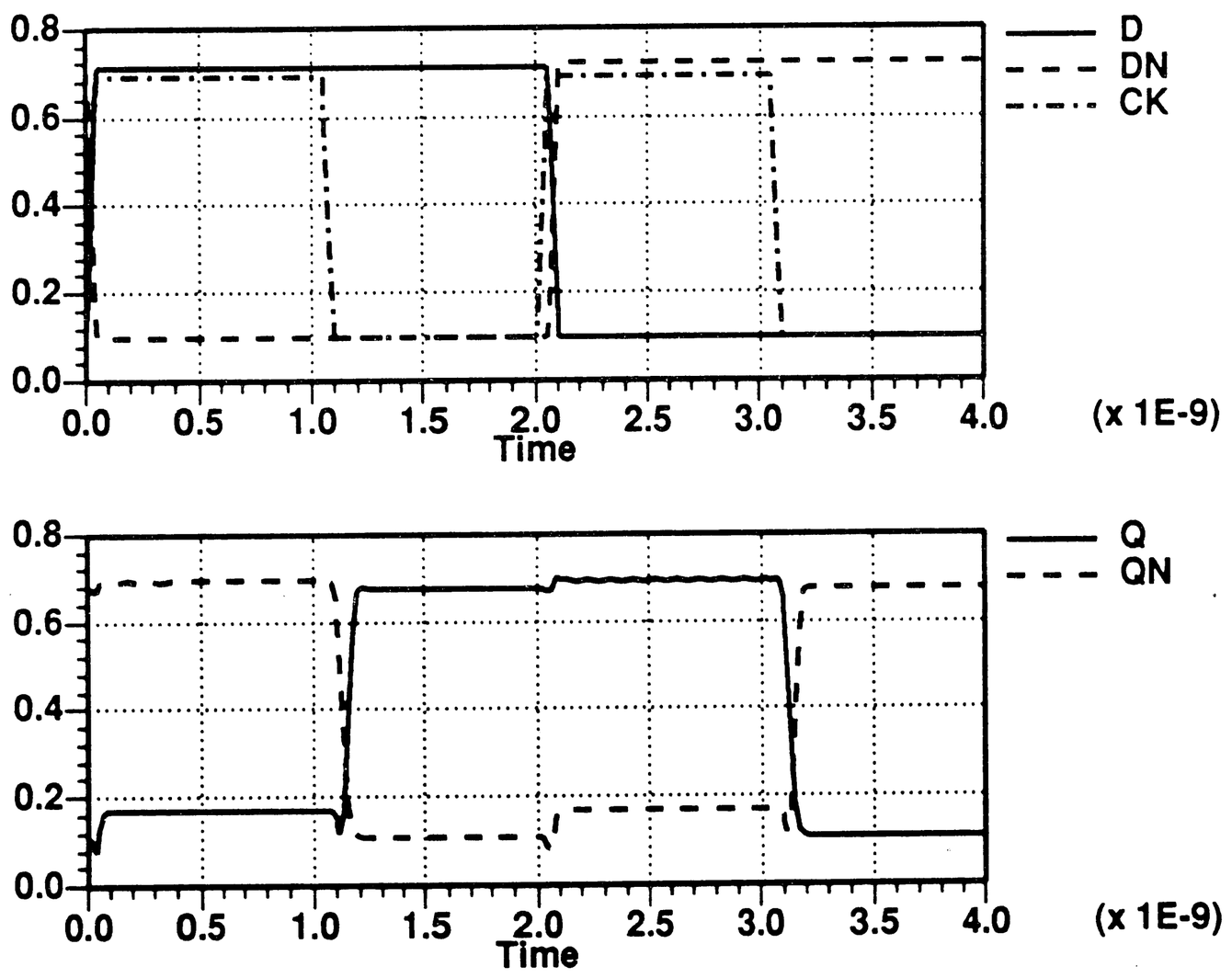
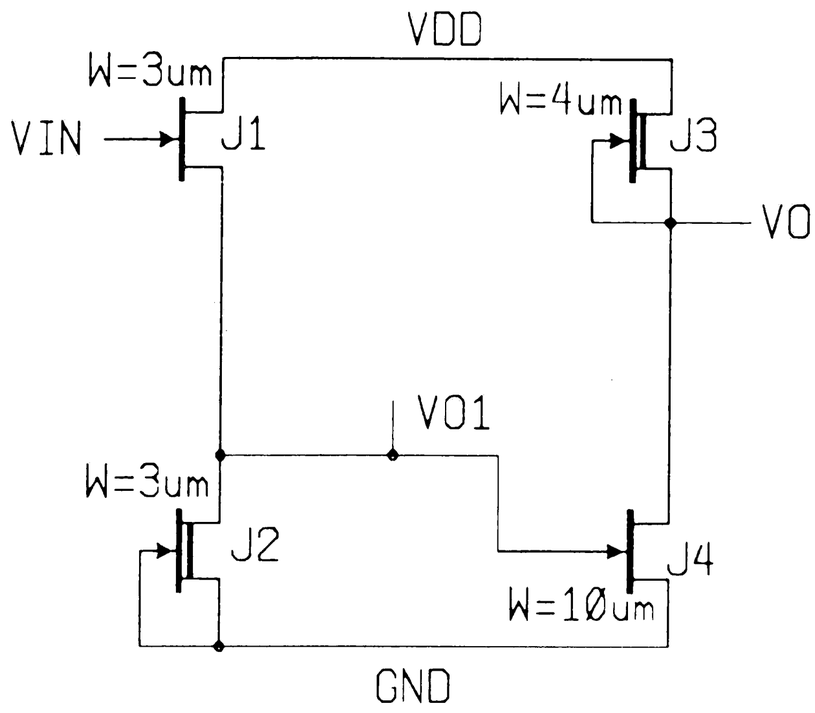
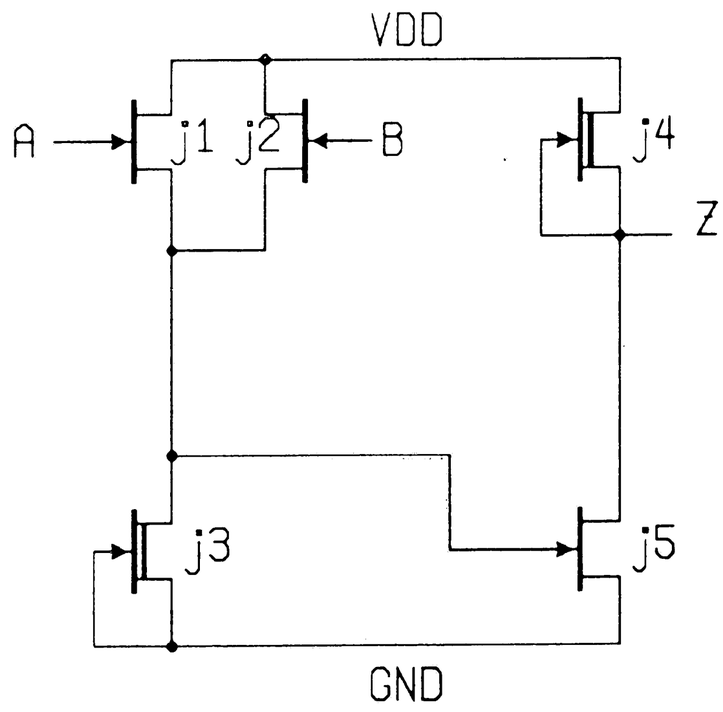


Figure 4.7. DCFL clocked latch response.



(a)



(b)

Figure 4.8. (a) SFL inverter, (b) SFL NOR gate.

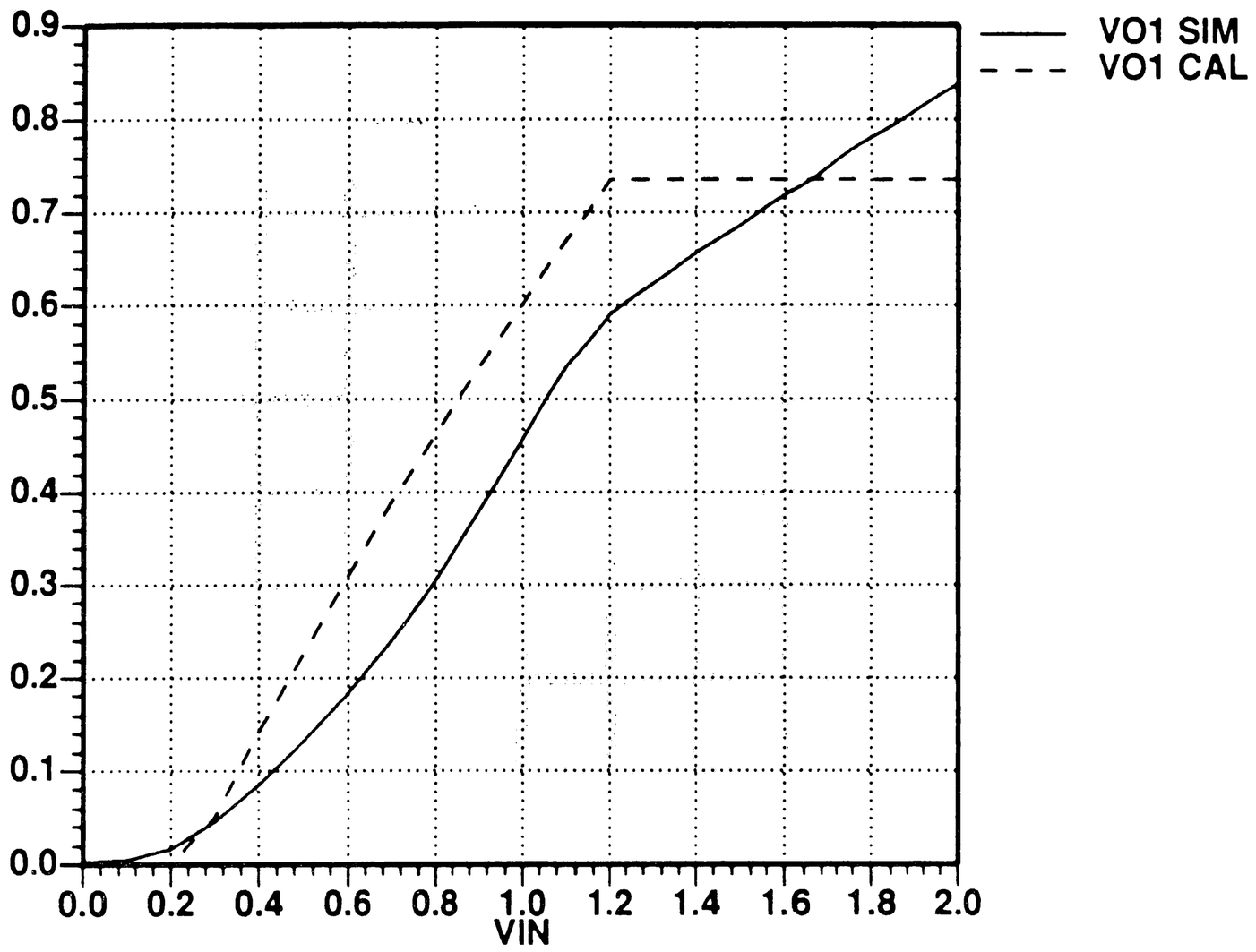


Figure 4.9. Source follower simulated and calculated transfer characteristics.

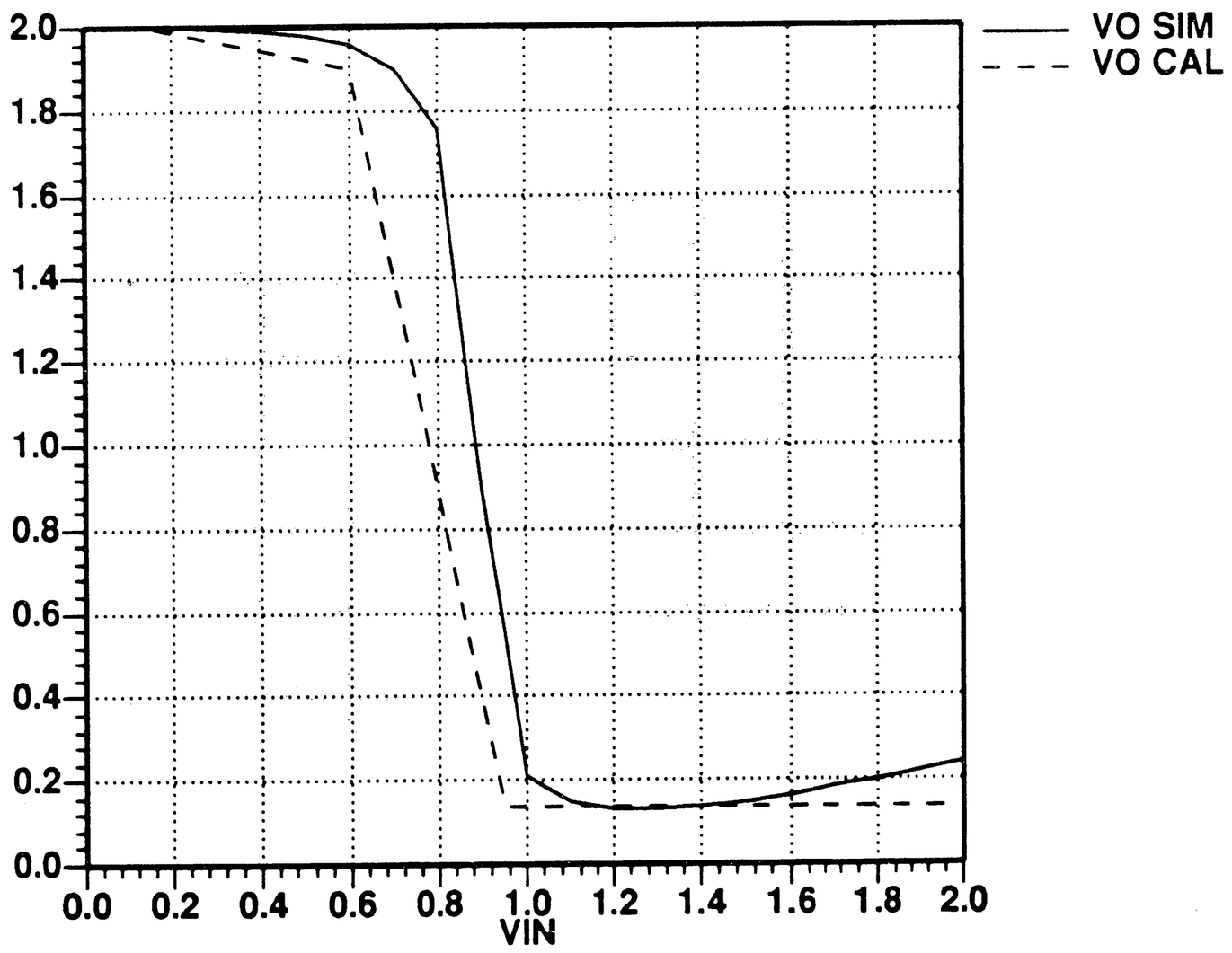


Figure 4.10. Simulated and calculated unloaded SFL transfer characteristics.

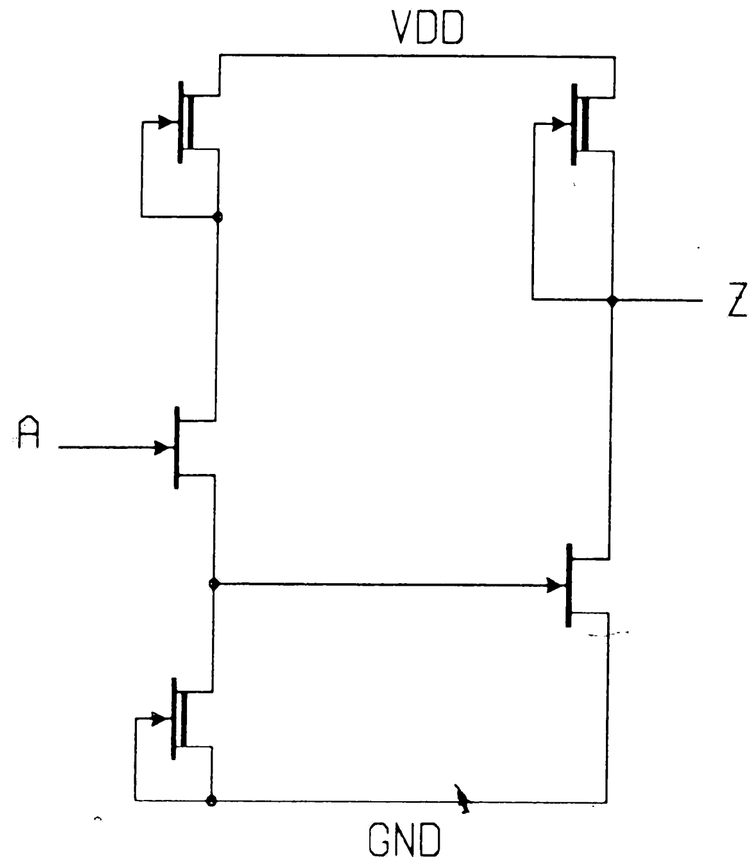


Figure 4.11. New SFL gate.

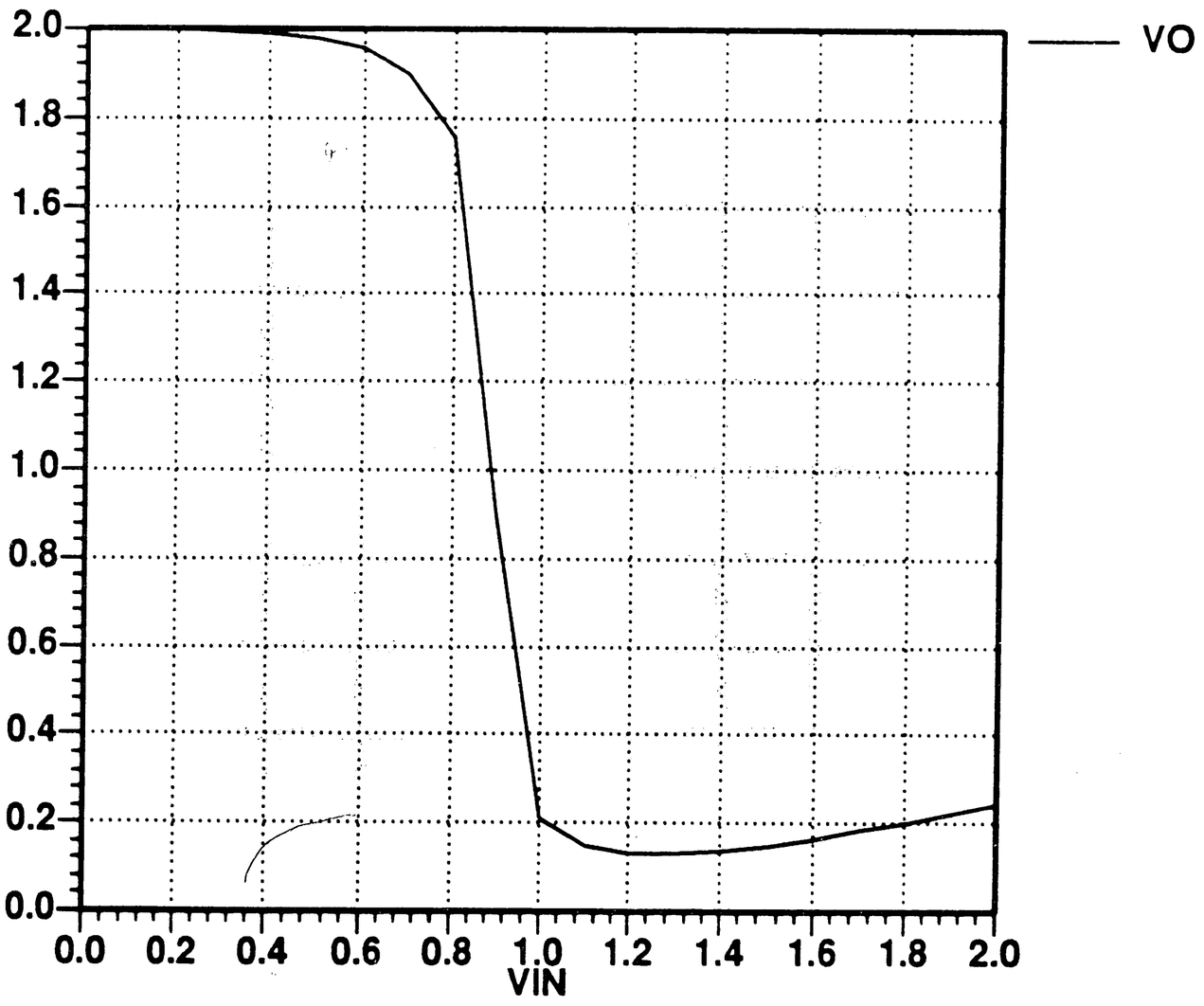


Figure 4.12. New SFL simulated unloaded transfer curve.

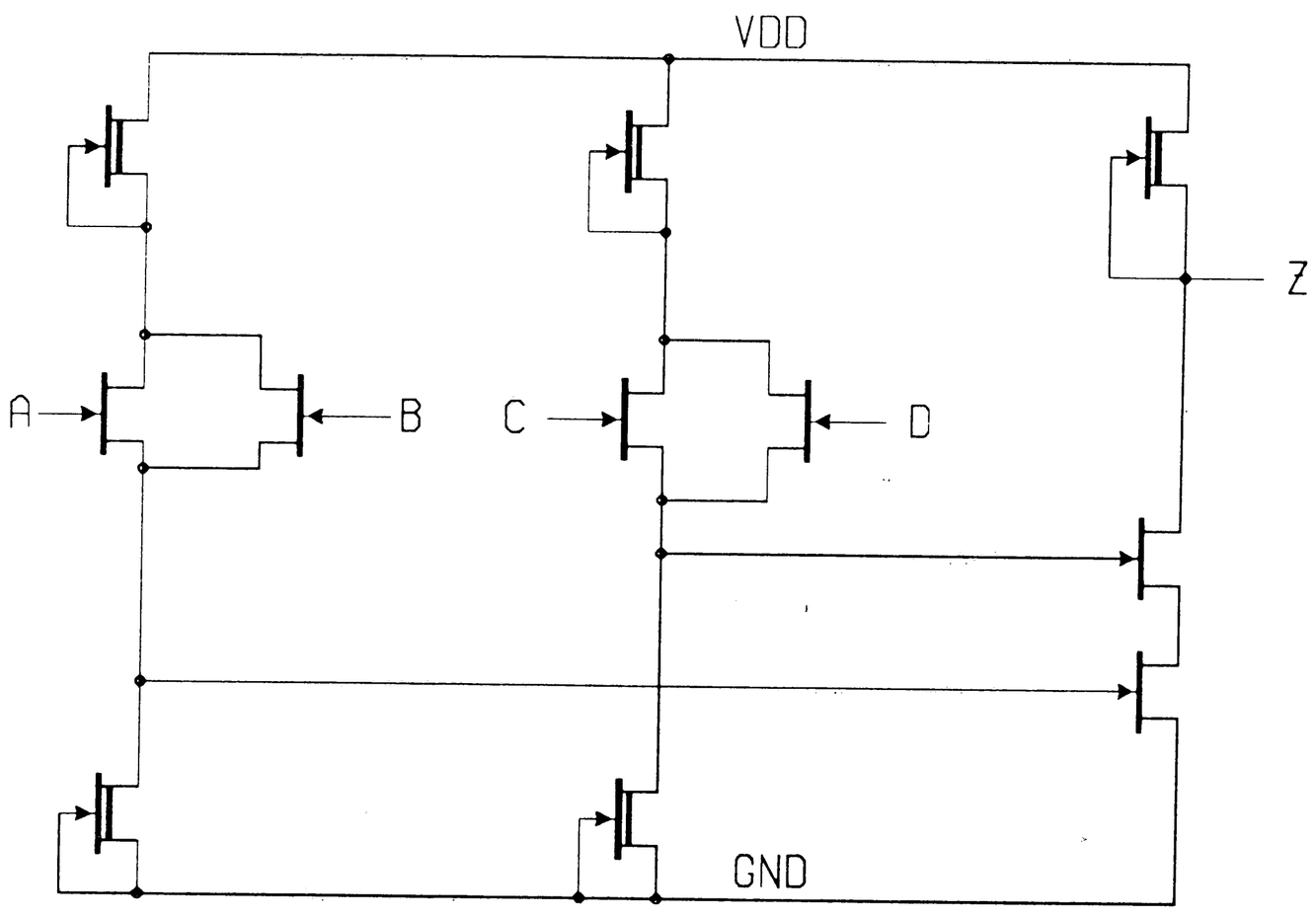


Figure 4.13. SFL OR/AND/INVERT gate.

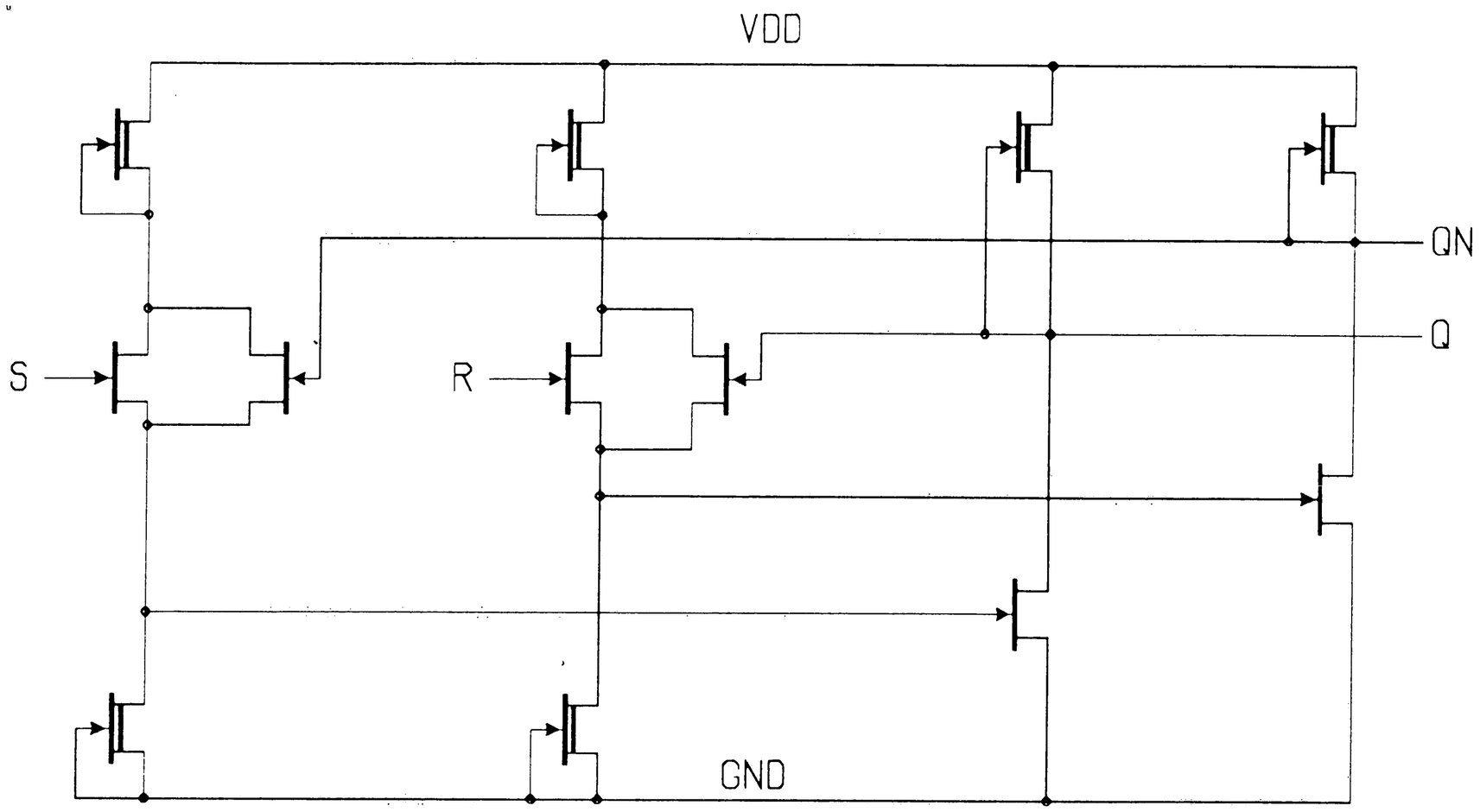


Figure 4.14. SFL SR latch.

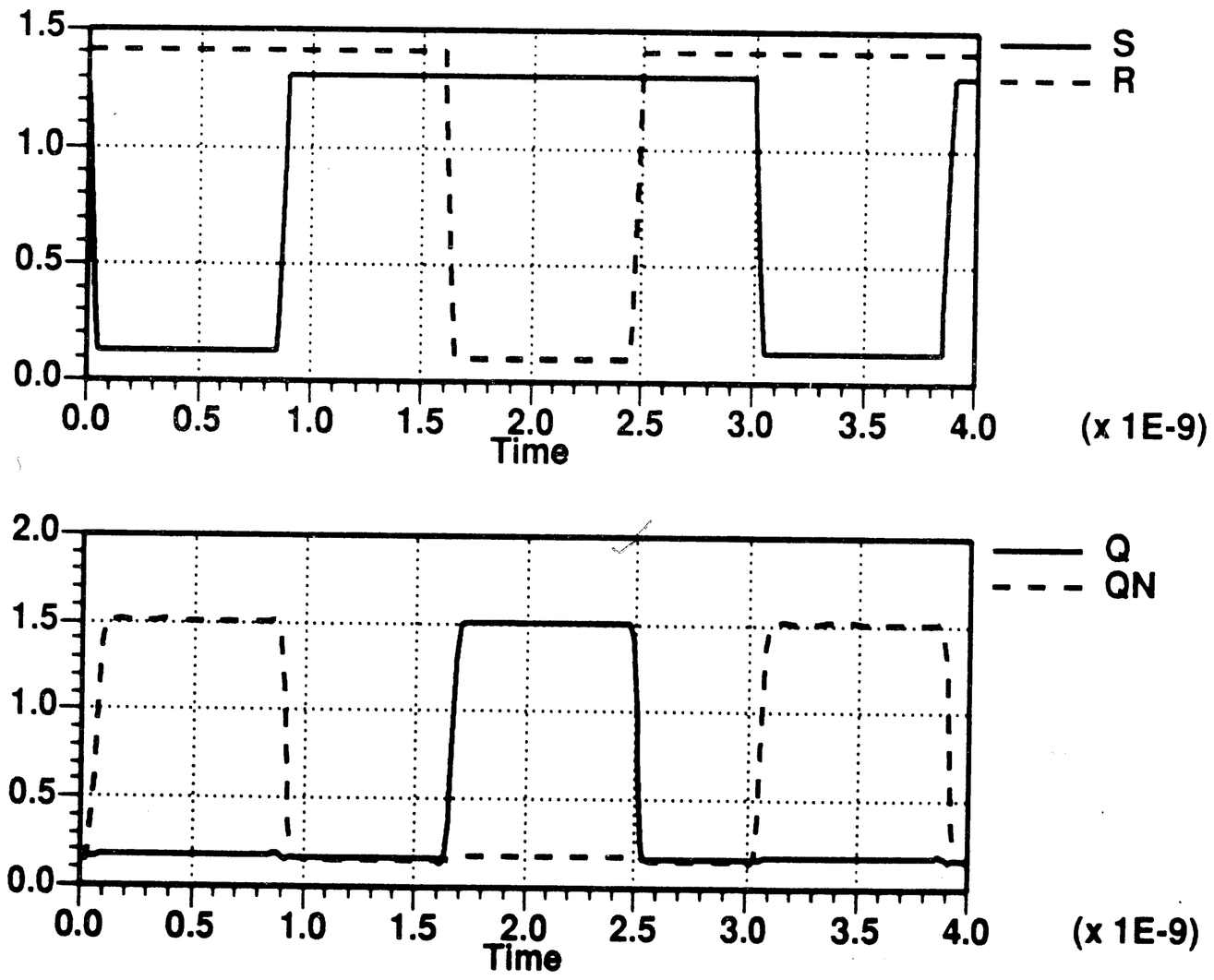


Figure 4.15. SFL SR latch response.

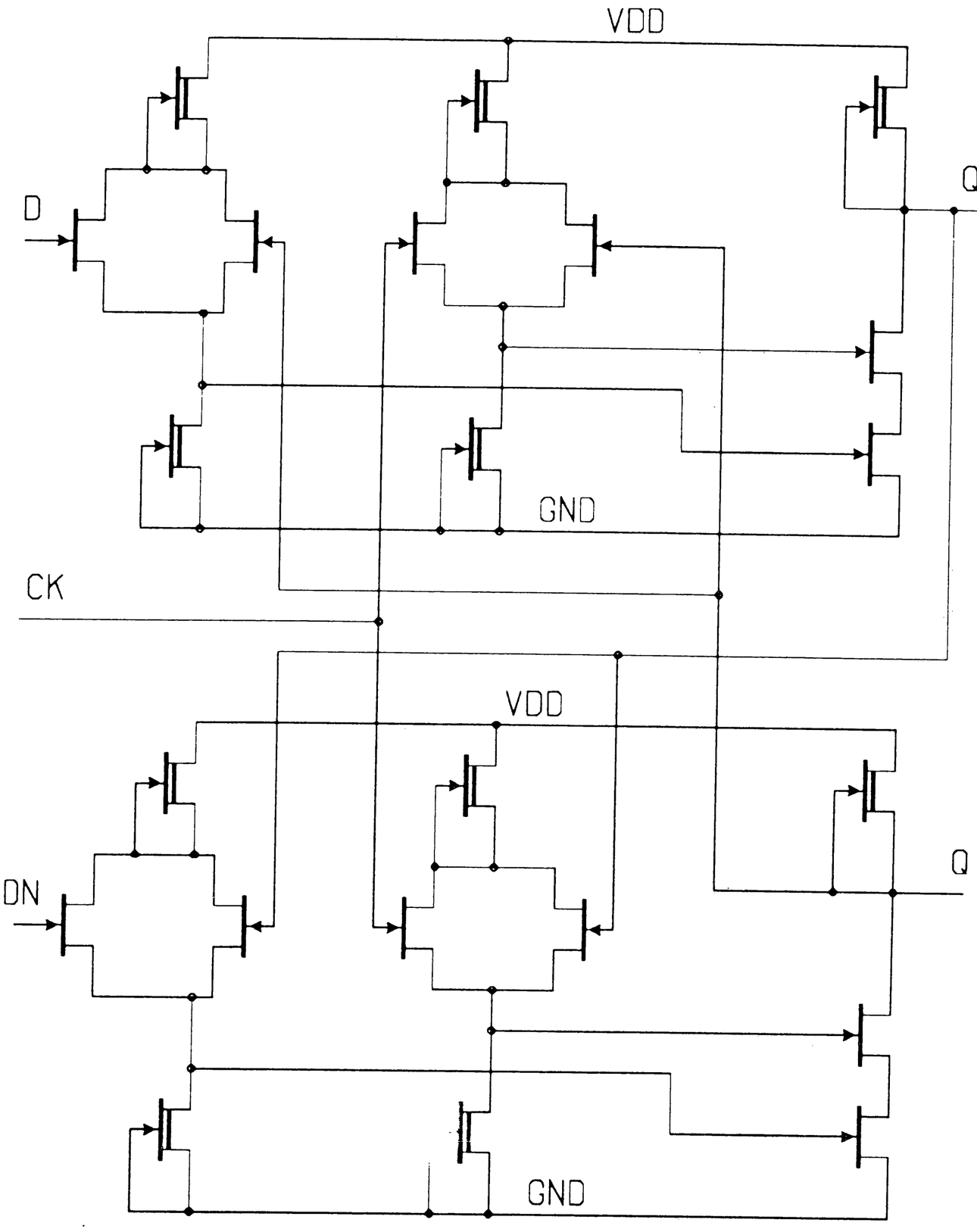


Figure 4.16. SFL Clocked latch.

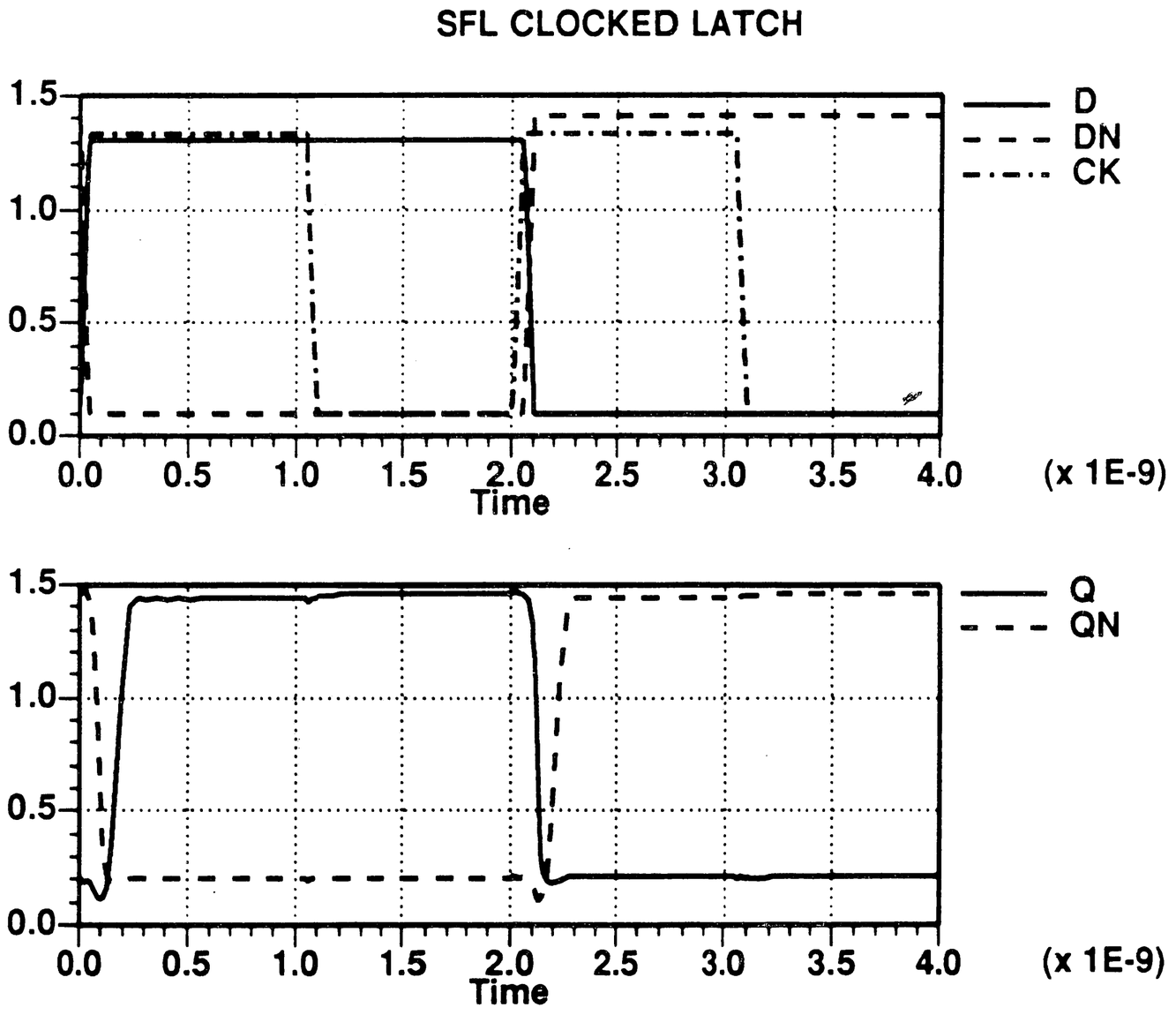


Figure 4.17. SFL clocked latch response.

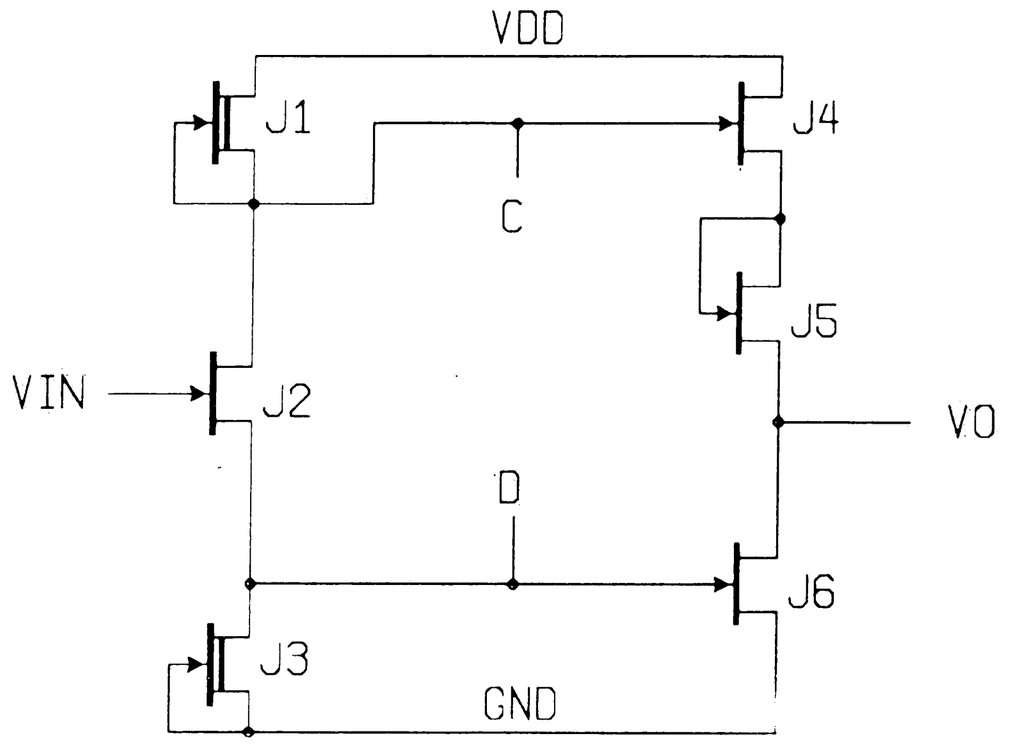


Figure 4.18. Push/Pull SFL inverter.

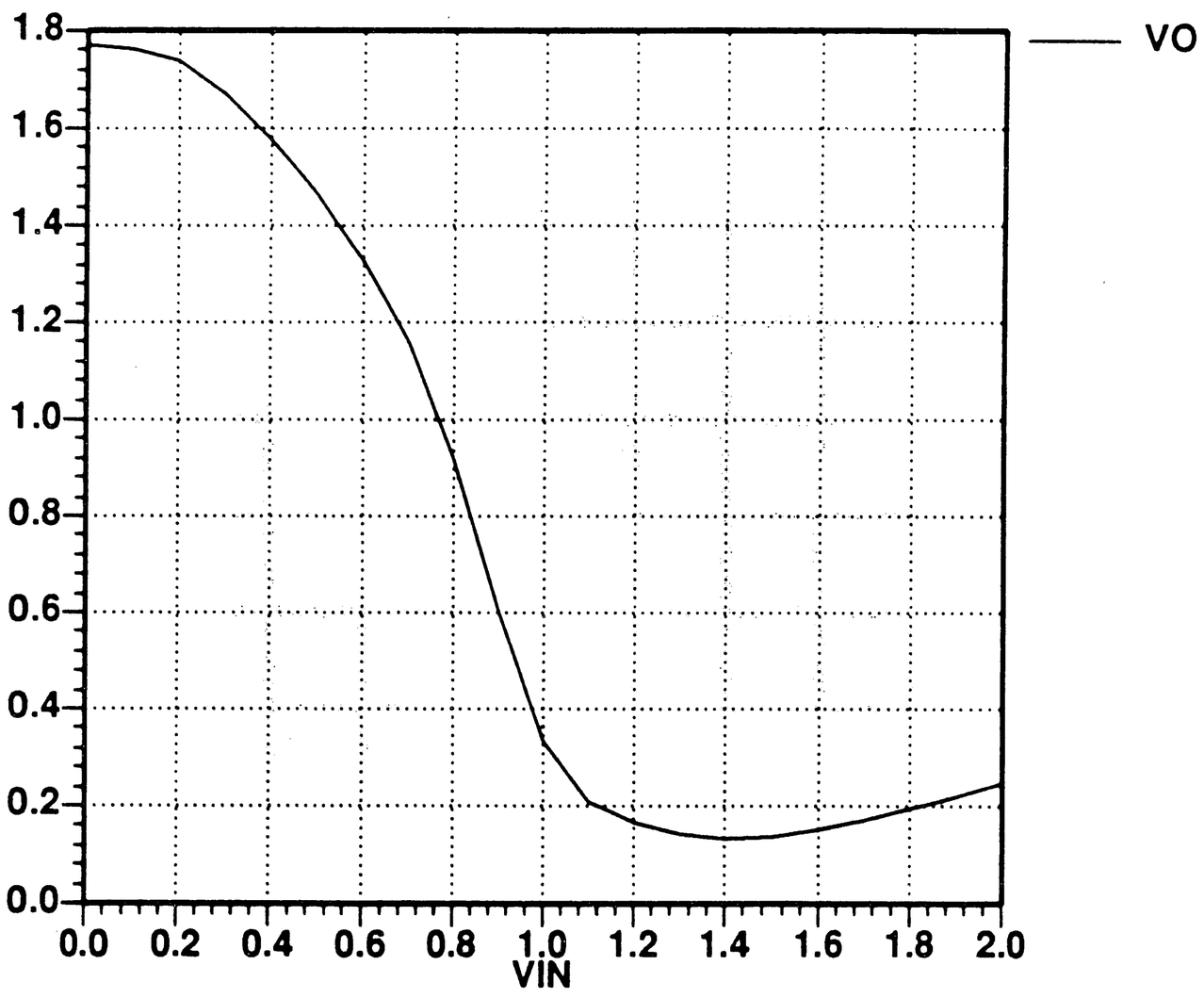


Figure 4.19. Push/Pull SFL unloaded transfer curve.

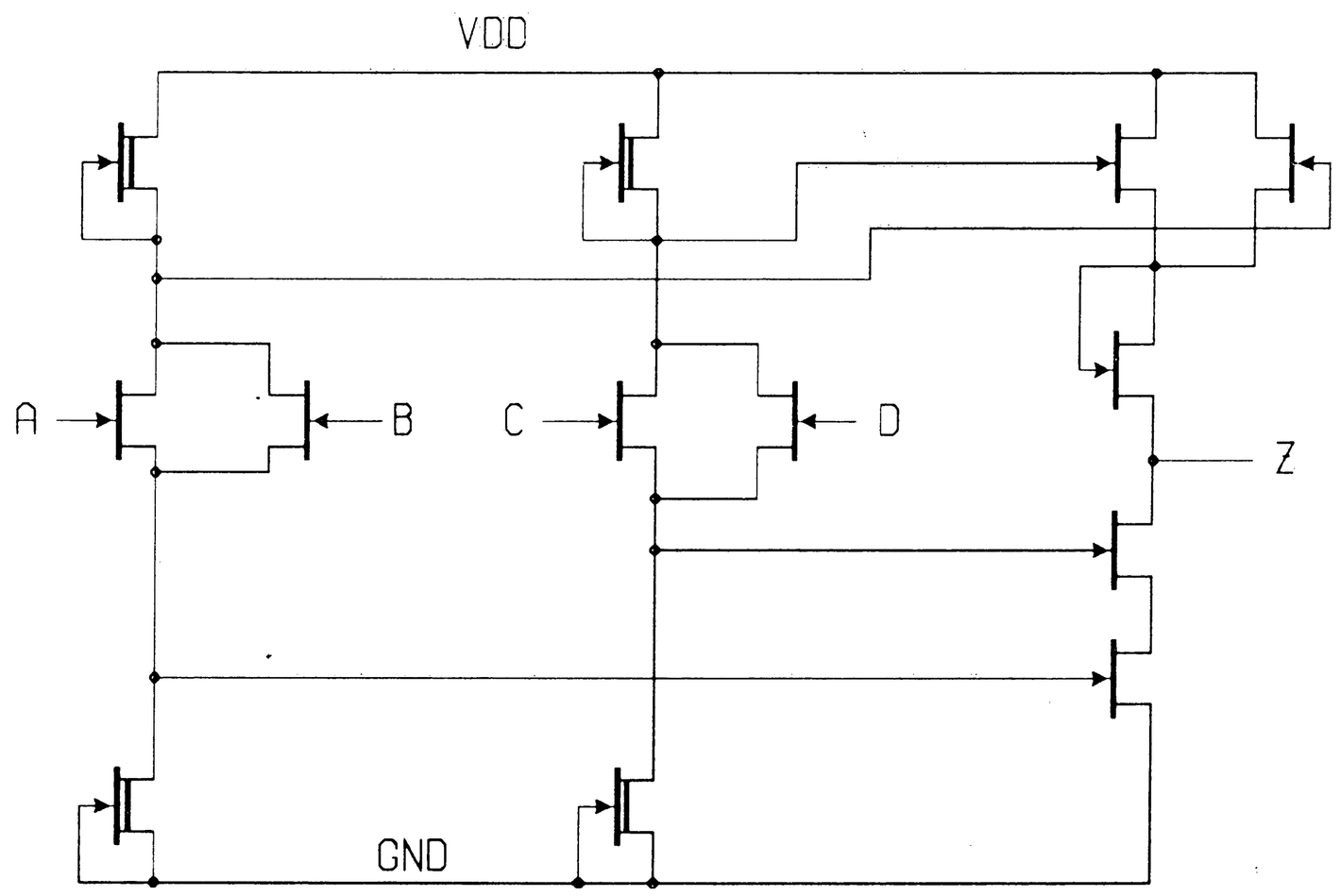


Figure 4.20. Push/Pull SFL OR/AND/INVERT gate.

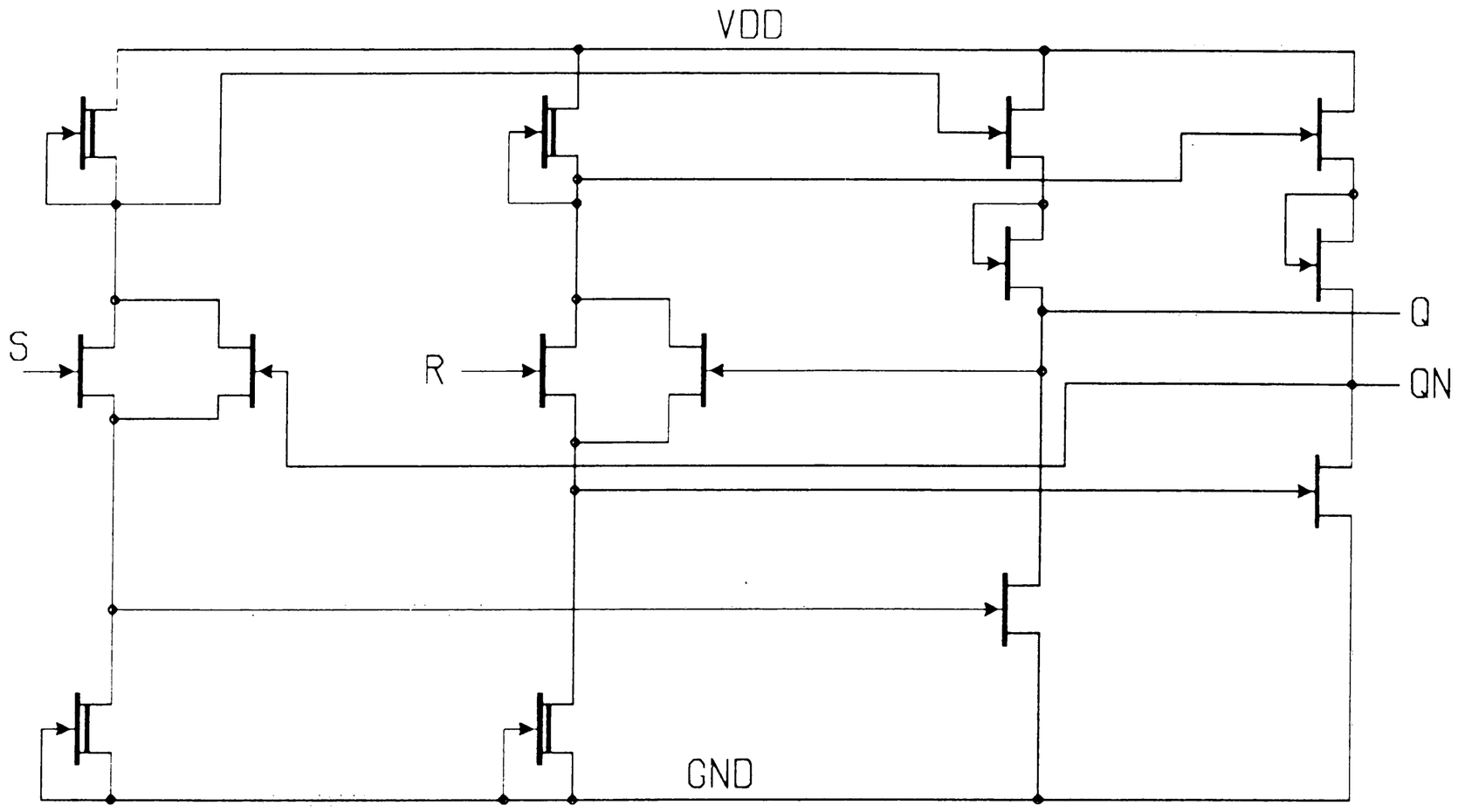


Figure 4.21. Push/Pull SFL SR latch.

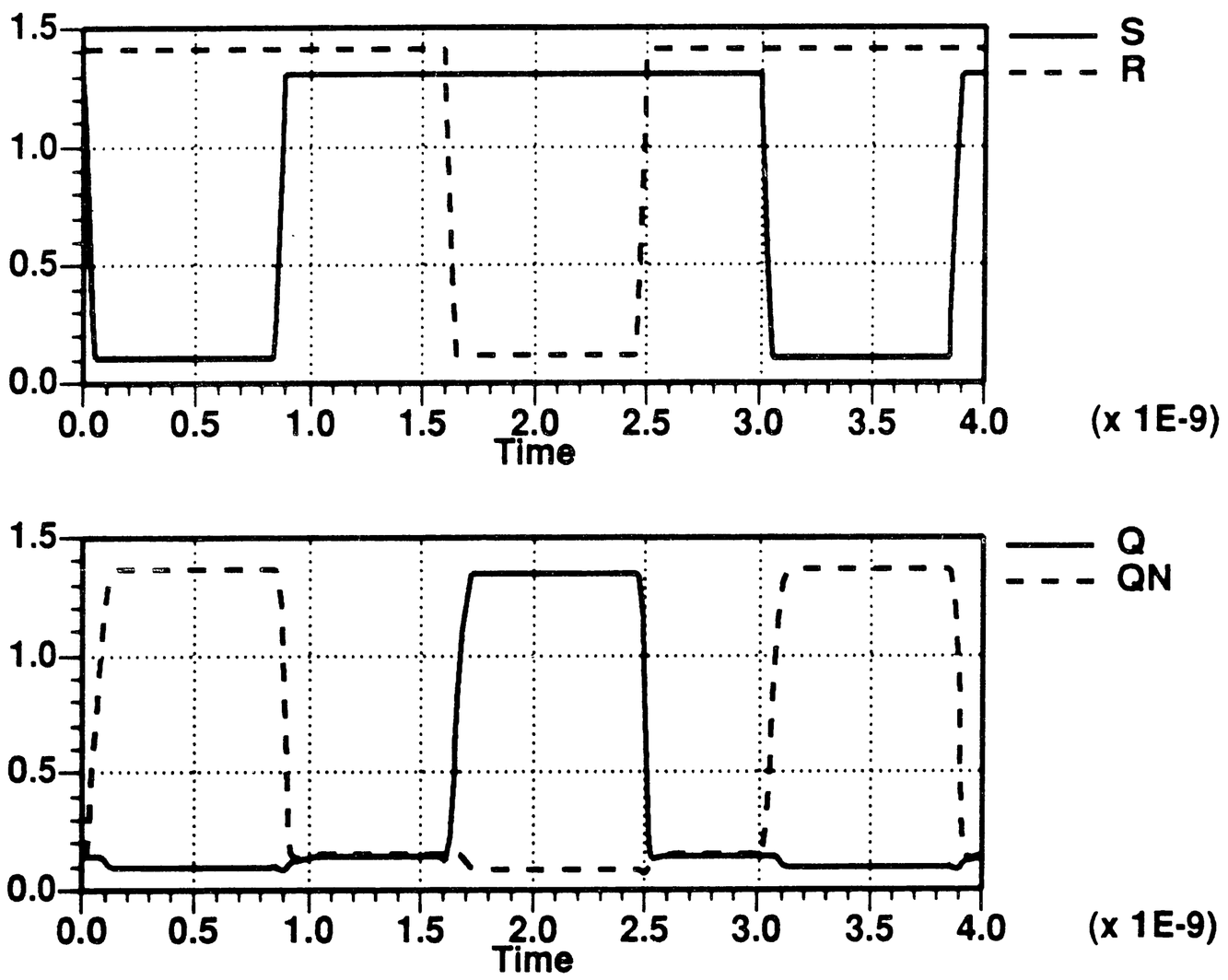


Figure 4.22. Push/Pull SFL SR latch response.

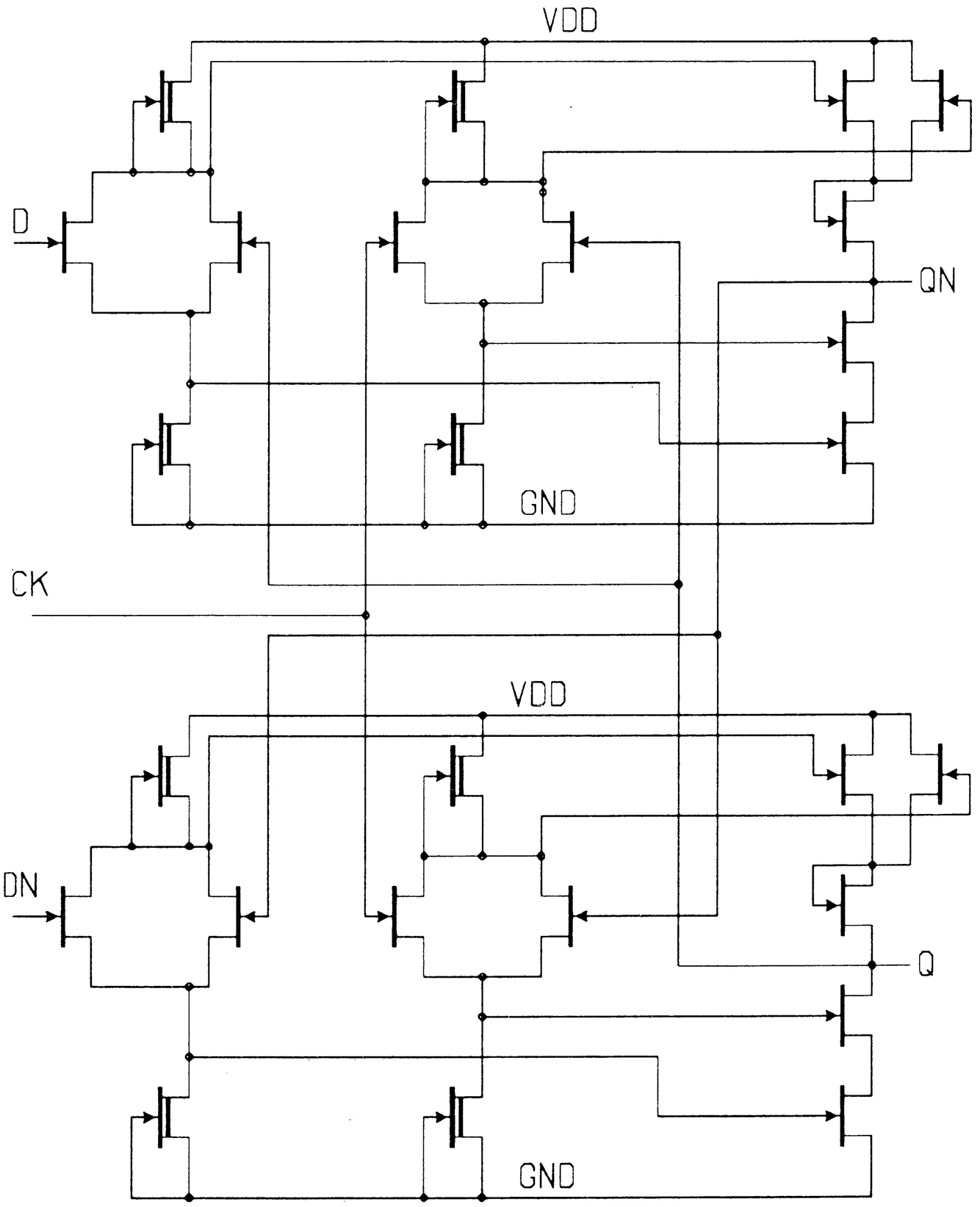


Figure 4.23. Push/Pull clocked SFL latch.

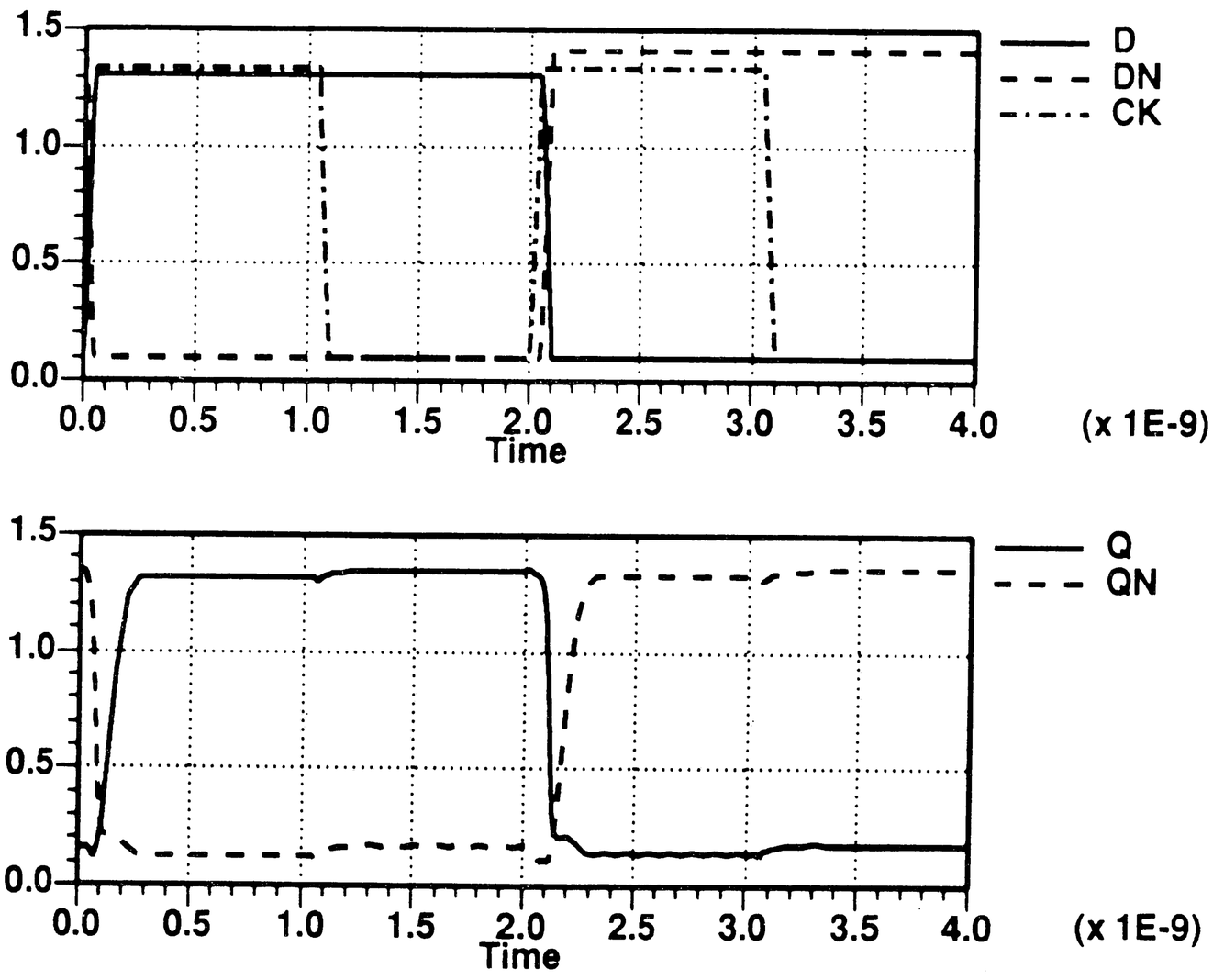


Figure 4.24. Push/Pull clocked SFL latch response.

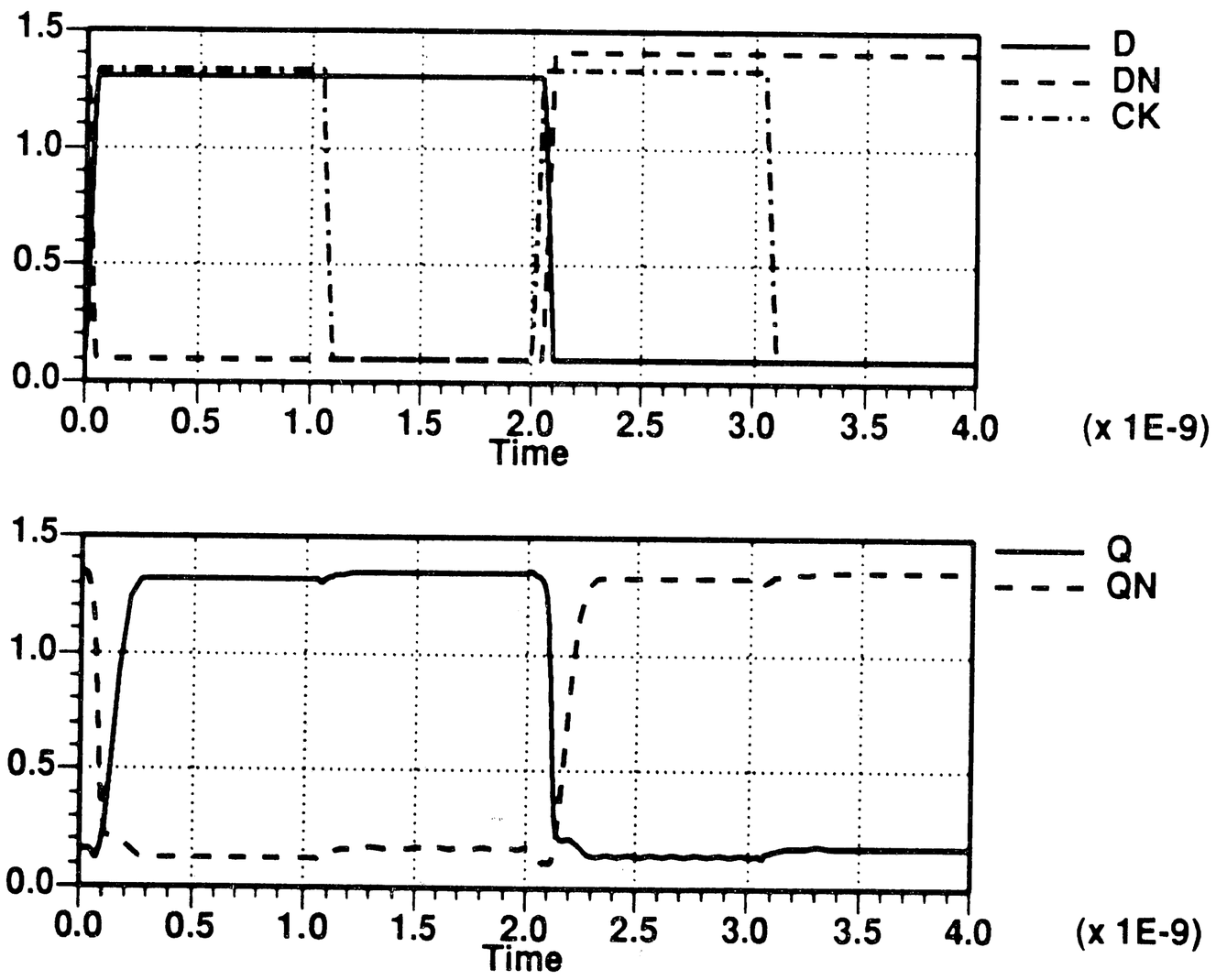


Figure 4.24. Push/Pull clocked SFL latch response.

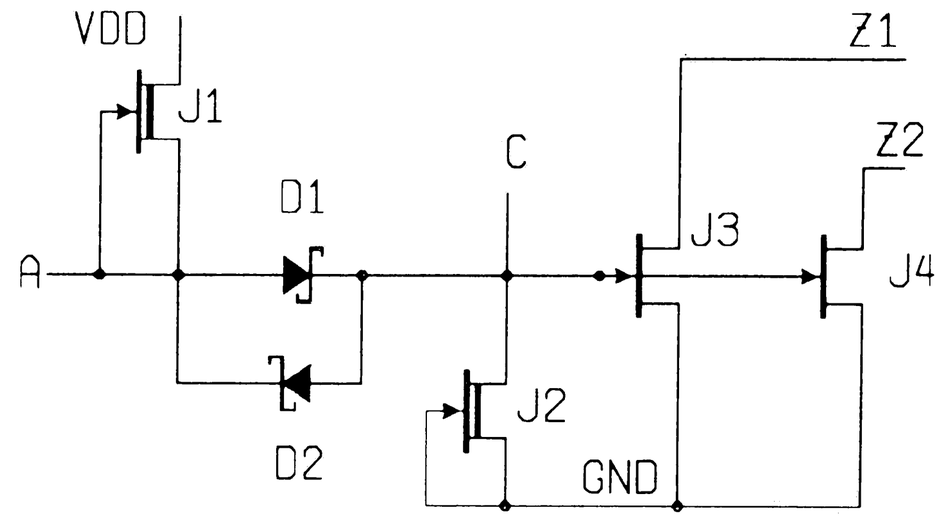


Figure 4.25. FIL inverter.

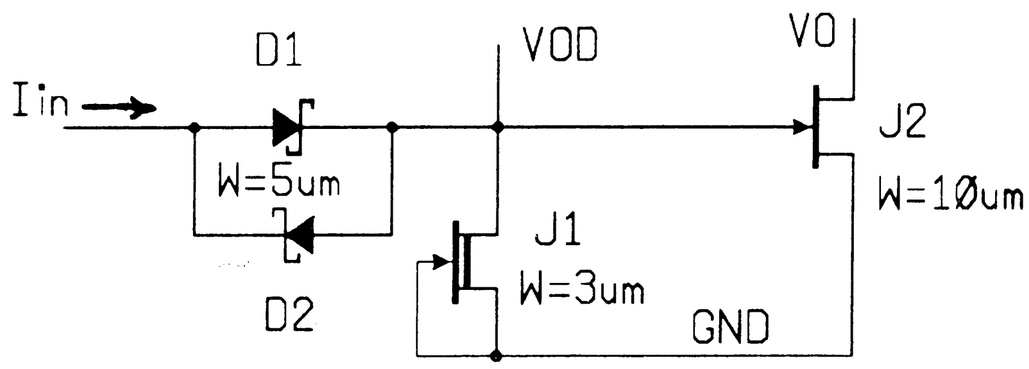


Figure 4.26. Simplified FIL inverter.

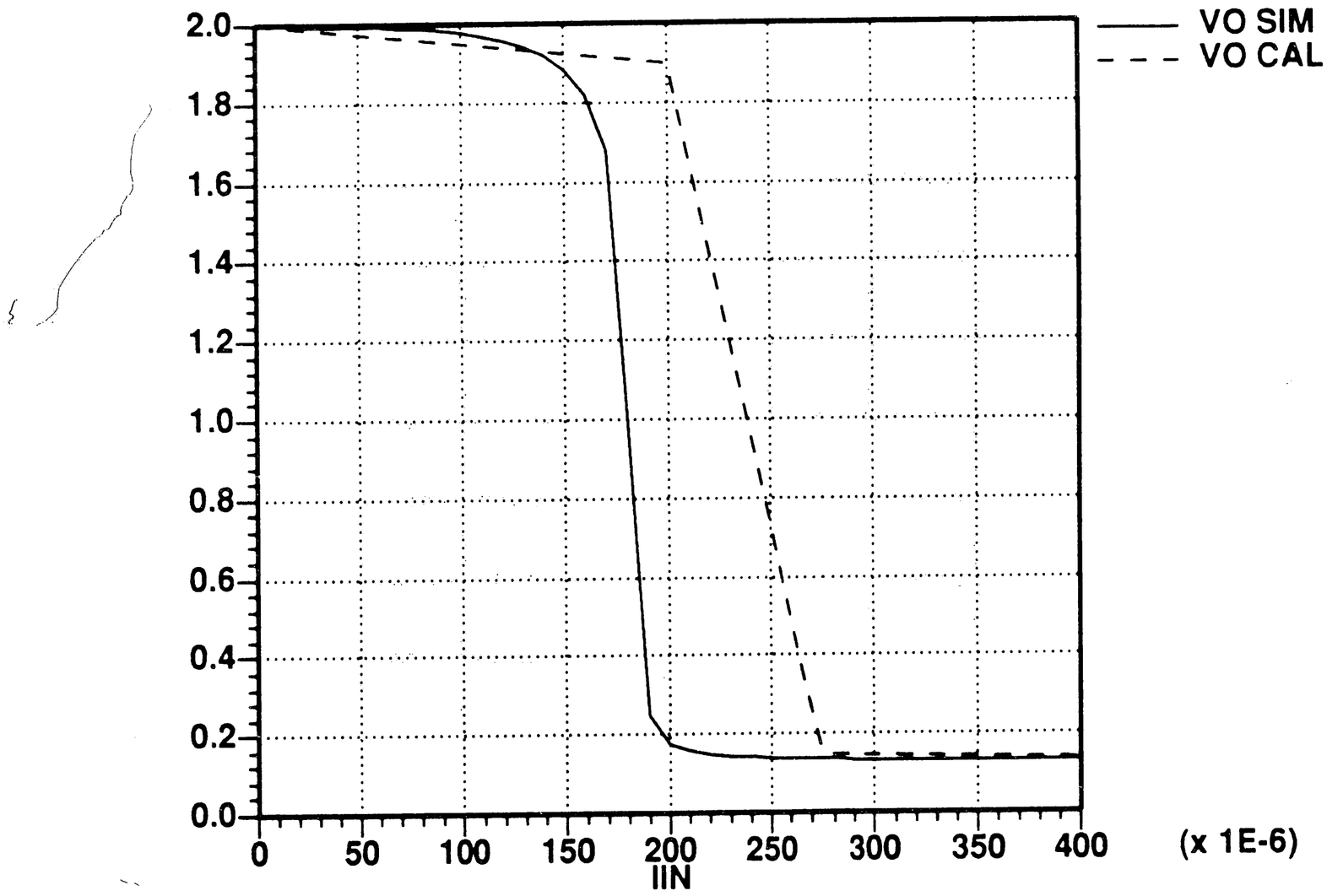


Figure 4.27. Calculated and simulated FIL unloaded transfer curve.

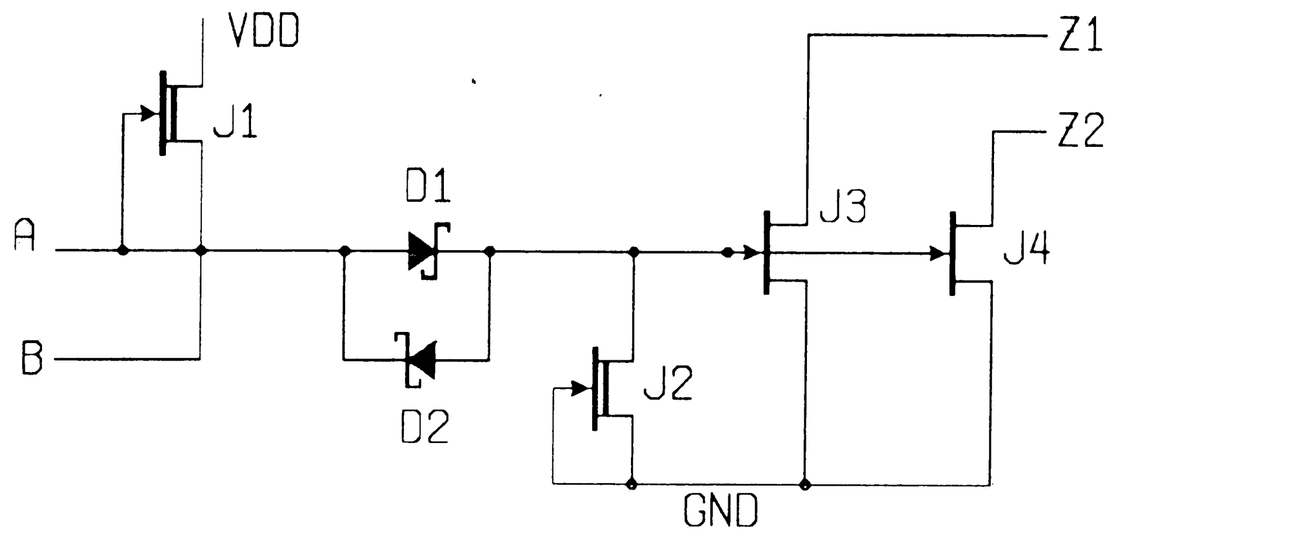


Figure 4.28. FIL 2 input NAND gate.

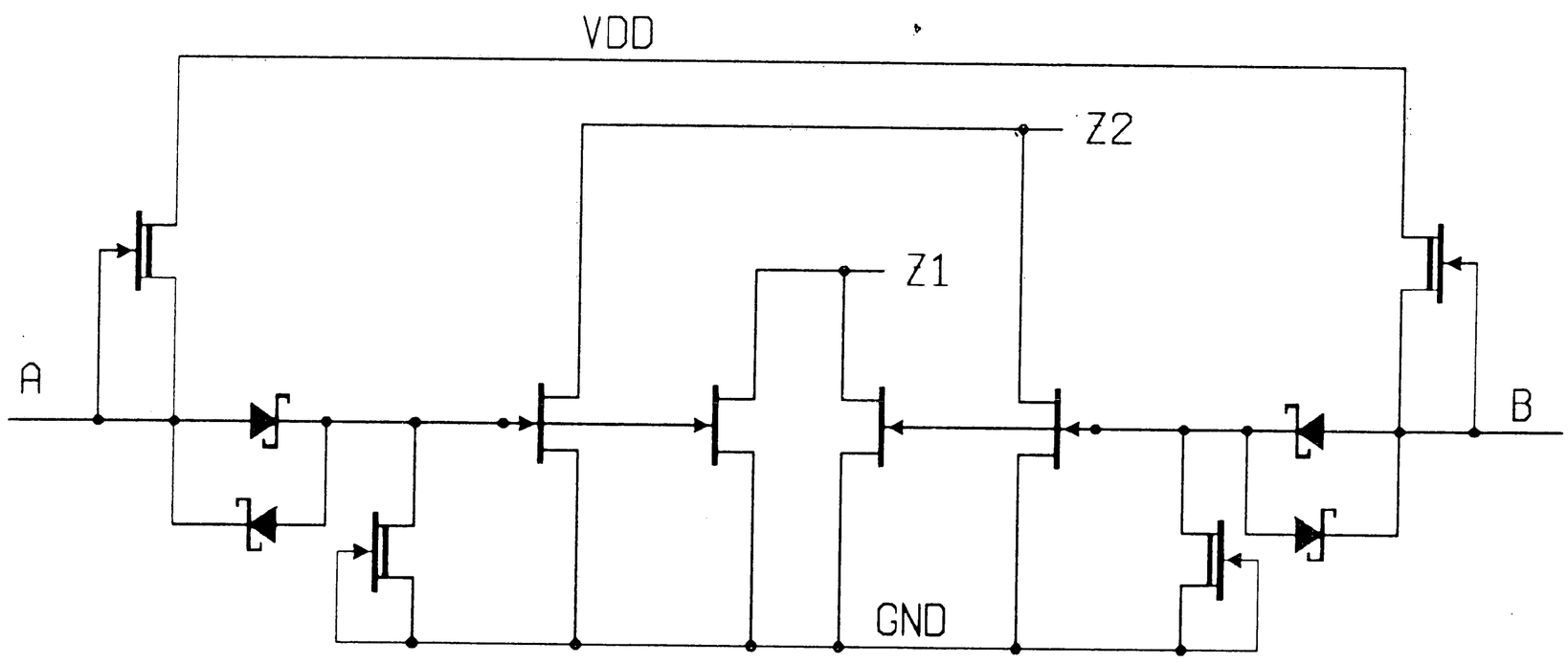


Figure 4.29. FIL 2 input NOR gate.

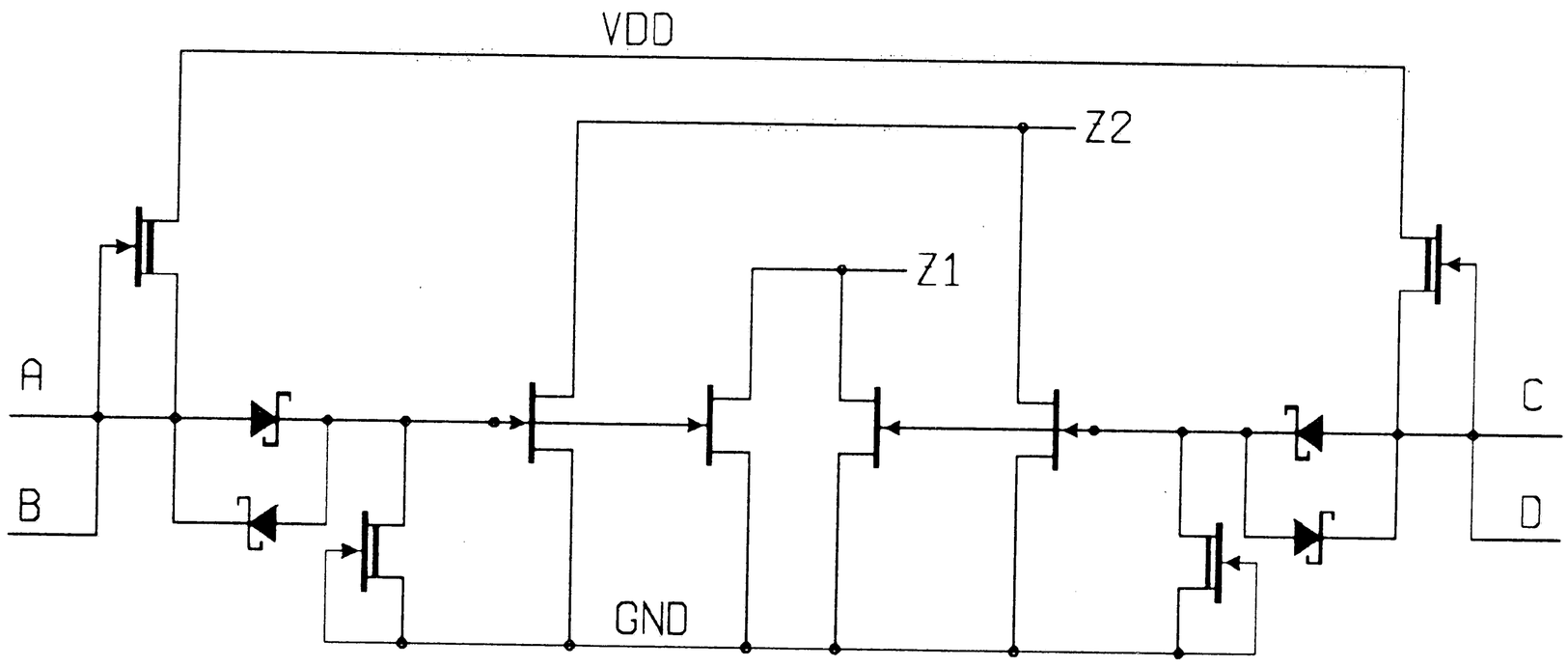


Figure 4.30. FIL AND/OR/INVERT gate.

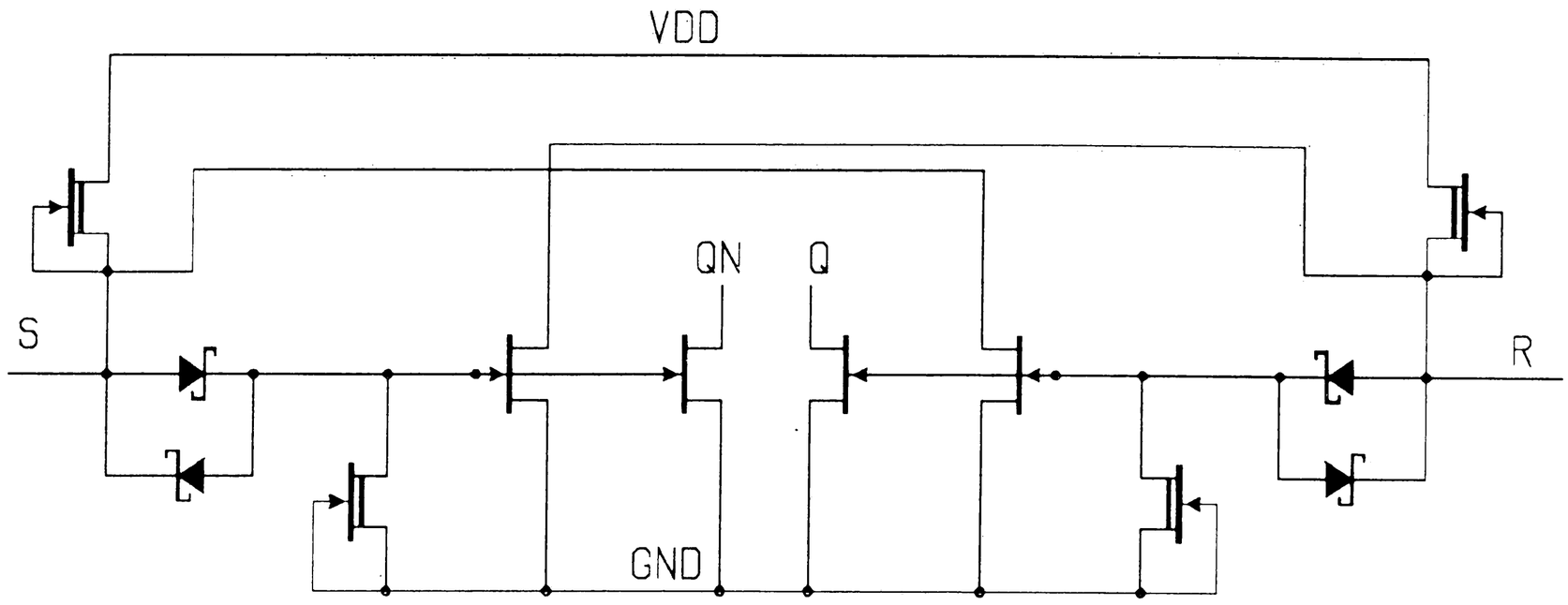


Figure 4.31. FIL SR NAND latch.

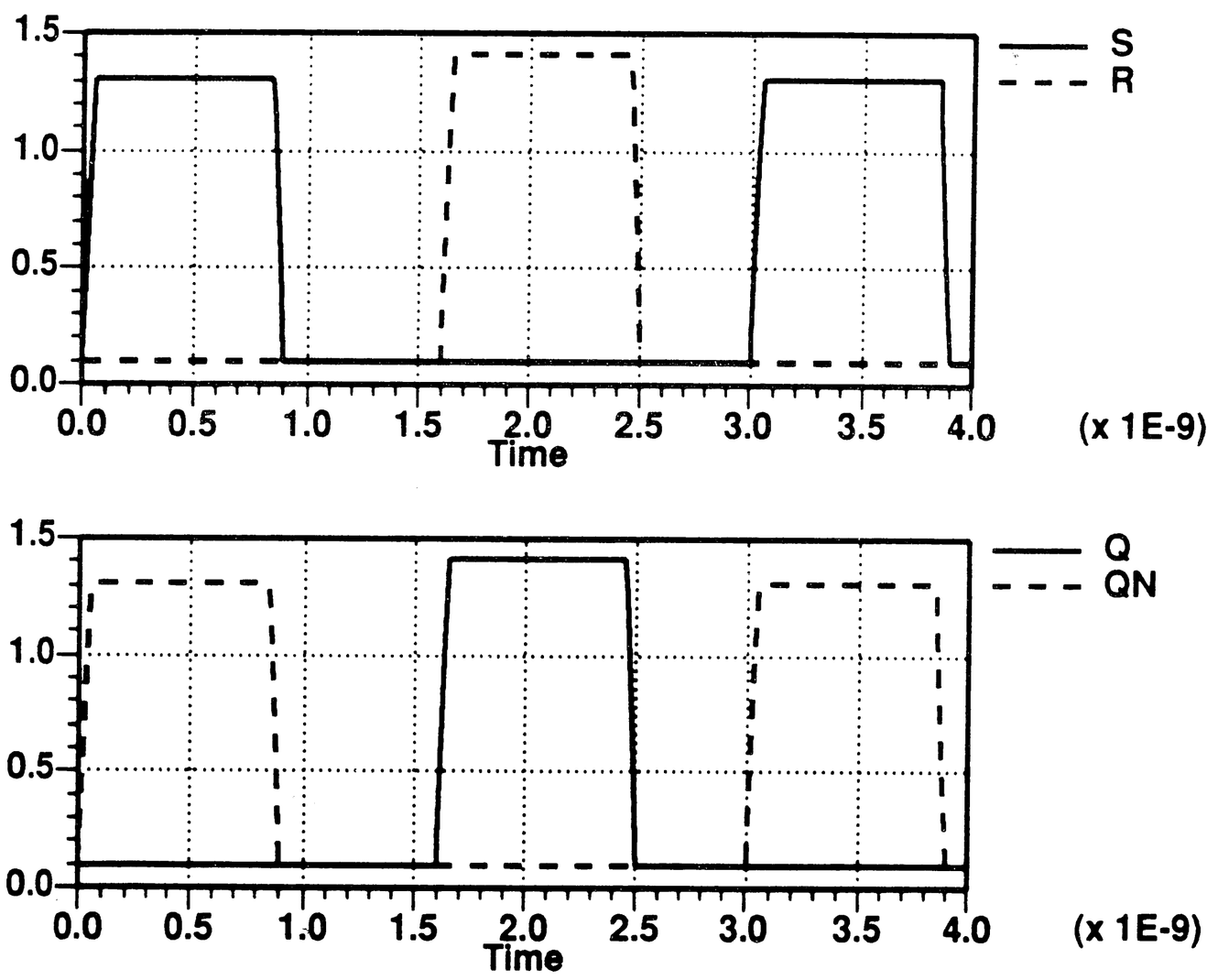


Figure 4.32. FIL SR latch response.

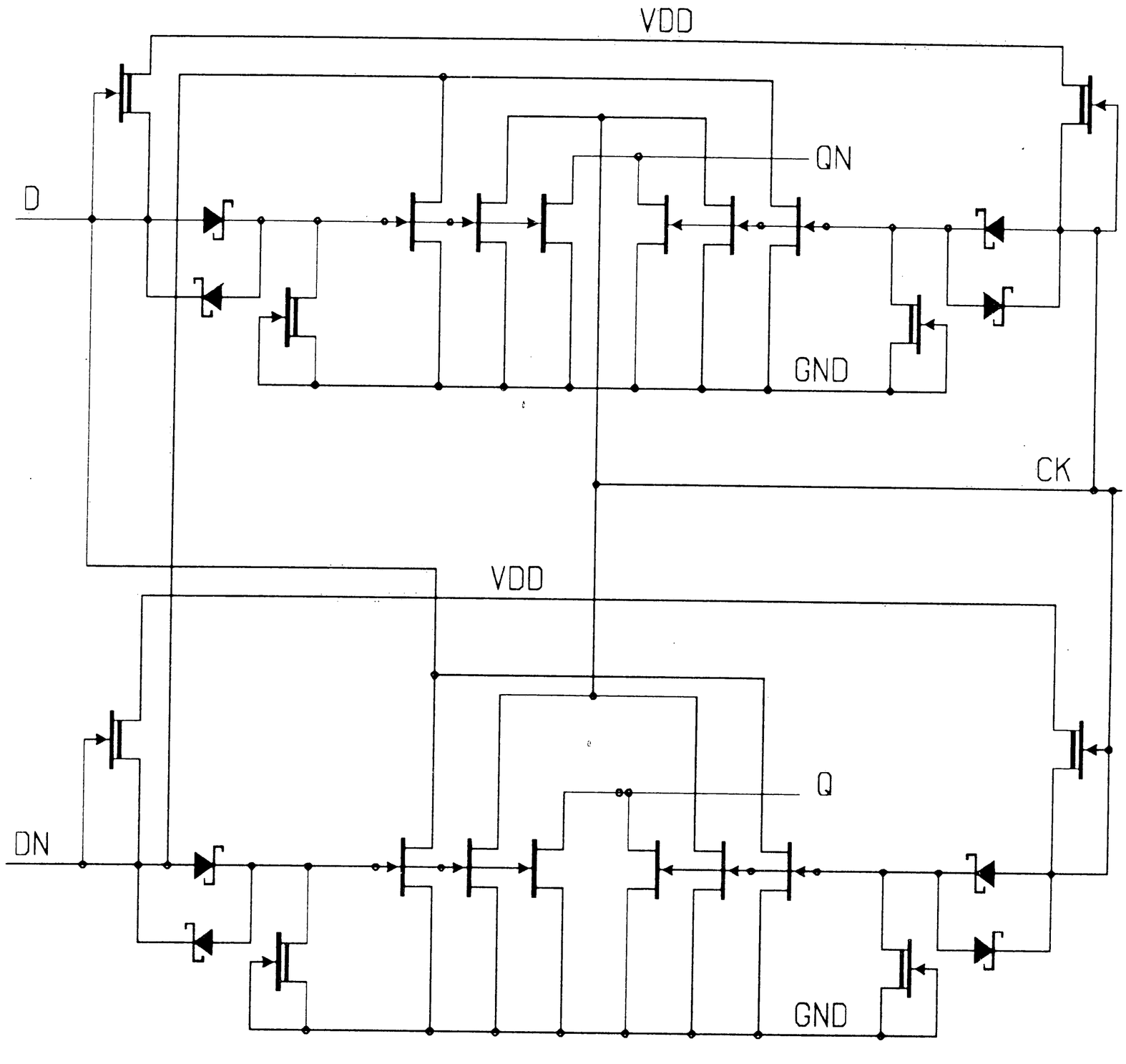


Figure 4.33. FIL clocked complex latch.

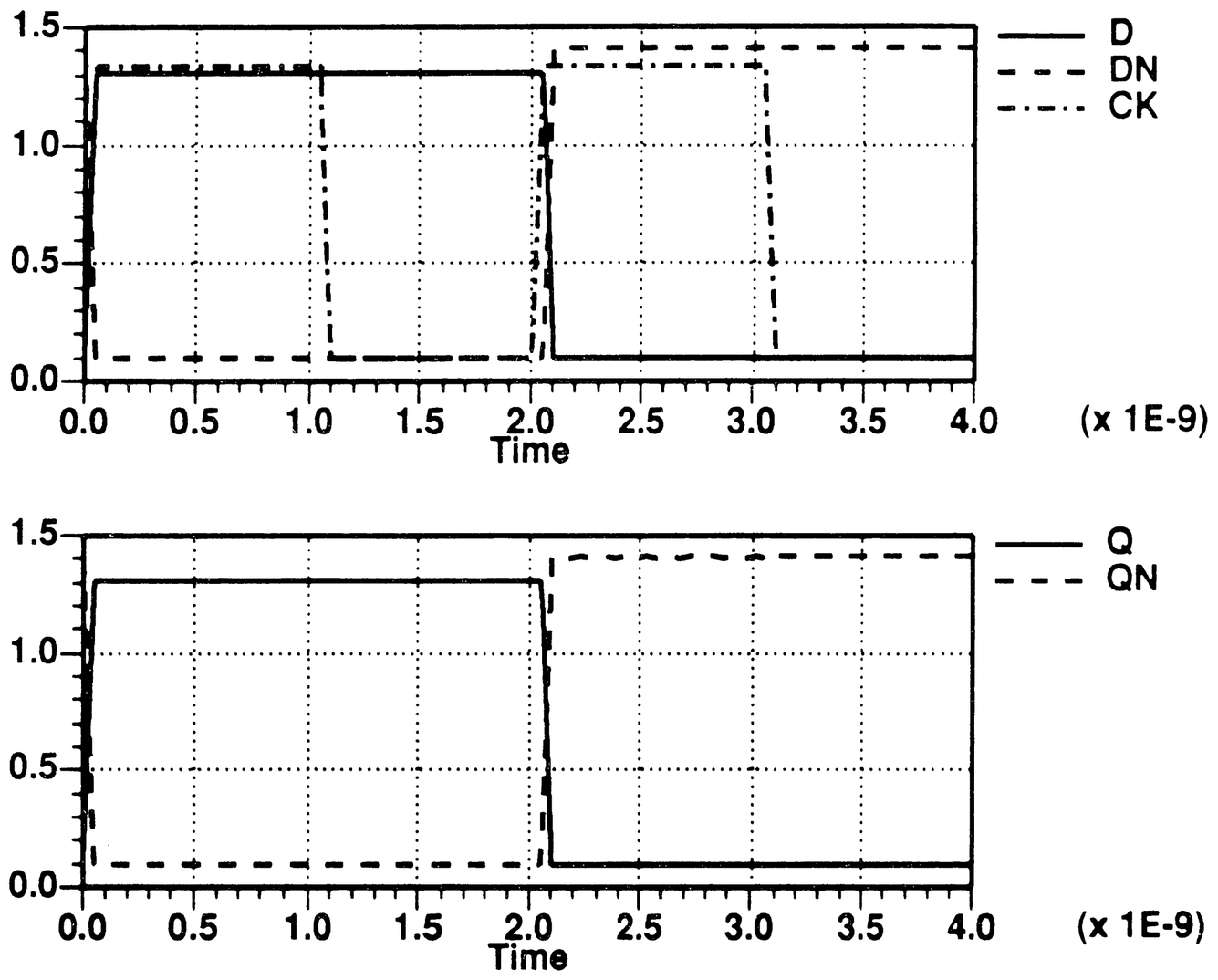


Figure 4.34. FIL clocked latch response.

CHAPTER 5

SIMULATION RESULTS

5.1. Family Characterization

Digital GaAs integrated circuits are primarily designed using logic gates, since the use of pass transistor logic in GaAs is not feasible due to the parasitic Schottky diode of a GaAs FET. Synthesis using logic gates requires complete understanding of the characteristics of the logic families used and their impact on circuit yield with a given process. The digital circuit designer is primarily interested in the DC noise margins versus fanin and fanout, the AC noise margin, and fanin/fanout loading of a logic family along with the power dissipation.

The behavior of a logic family must also be understood as a function of temperature, since a small LSI chip in GaAs can easily dissipate a few watts excluding I/O power. Temperature constraints are very severe in GaAs technology due to the very low noise margins, especially since device threshold voltages vary as much as 150 mV versus temperature. This is extremely important since noise margins are on the order of 0.5V or less at 25° C for most GaAs logic families.

Each of the logic families discussed is characterized for DC and AC characteristics at 25 and 125° C. DC analysis of noise margins is performed on 3 input NOR or NAND gates as a function of fanin for a fanout of 3. The AC analysis is

performed on 7 stage 3-input NOR/NAND gate ring oscillators. The logic families are characterized in AC mode for AC noise margins and driving capability versus fanout and wire capacitance. This analysis is done for gates with one input driven (fanin=1) and 3 inputs driven (fanin=3).

The logic families were sized as to maintain a power dissipation below 700 μW at a power supply voltage of 2.0 V. The logic families have been simulated using AT&T's ADVICE circuit simulator. The ADVICE simulator uses a general purpose HFET model with a model parameter set as shown in the device characteristics section of Chapter 3. The simulations are done at 25 and 125° C using nominal, low, and high EFET to DFET drain current ratios.

5.2. Simulation Set-up

Seven stage ring oscillator structures were laid out using AT&T's SARGIC GaAs process with 1 μm gate length and 2 μm width, and spacing double level metal process to characterize the logic families. The logic families are characterized by ring oscillator simulations for AC noise margins, power dissipation, and fanin/fanout sensitivity. Gate delays are calculated by measuring the center frequency of oscillation and using Equation 5.1.

$$t_p = 1/(2\ f_o\ N) \qquad (5.1)$$

where t_p is the propagation delay, f_o is the oscillator center frequency, and N is the number of oscillator gates. Each logic family is characterized for DC noise margins for a fanin of 1 and 3 to measure noise margin degradation. This analysis is performed at 25 and 125° C using the nominal, high, and low models.

Ring oscillators with a fanin of one were simulated. The oscillators have fanouts of 1 and 4 loads for measuring the AC noise margins and the fanout sensitivity. Similar ring oscillators were set up with wire length of 200 and 500 μm of wire. This is equivalent to 45 and 110 femto Farads of capacitance for measuring wire load sensitivity. This set up is shown in Figures 5.1 and 5.2.

Next ring oscillators with a fanin of three were simulated. The oscillators have fanouts of 3 and 4 loads for measuring the AC noise margins and the fanout sensitivity. Similar ring oscillators were set up with wire length of 200 and 500 μm of wire. This is equivalent to 45 and 110 femto Farads of capacitance for measuring wire load sensitivity. This set up is shown in Figures 5.3 and 5.4. This analysis was also done at 25 and 125° C using the nominal, high, and low current EFET to DFET drain current ratios.

The AC noise margin were measured by varying the power supplies VDD2 and VSS2 relative to VDD1 and VSS1. The AC noise margin high is extracted by lowering VDD2 and VSS2 while maintaining 2 V across the gates until the oscillator

stalls. The change in VDD2 and VSS2 yields the AC noise margin high of the oscillator. Similarly the AC noise margin low is measured by raising VSS2 and VDD2 again maintaining 2 V across the gates until the oscillator stalls. The difference in power supply values yields the AC noise margin low of the gates. The AC noise margins high and low are expressed as follows:

AC NMH = |VDD2 - VDD1|

AC NML = |VSS2 - VSS1|

5.3 Direct Coupled FET Logic (DCFL)

A DCFL 3 input NOR gate schematic is shown in Figure 5.5, indicating the FET sizes in the ring oscillator layout. Figures 5.6 to 5.9 show the DC transfer characteristics for DCFL inverter at 25 and 125° C using the nominal, high, and low model parameters for FANIN=1 and FANIN=3. These figures are used in extracting the DC noise margins for DCFL. Figures 5.10 and 5.11 show the power delay product for a DCFL 3 input NOR gate with a FANIN and FANOUT of 3.

Tables 5.1 and 5.2 show DCFL characteristics for a FANIN of 1 and FANIN of 3 respectively. The tables show the simulated data for nominal, high, and low cases at 25 and 125° C.

TABLE 5.1. DCFL WITH FANIN = 1

	T = 25° C			T = 125° C		
	NOMINAL	HIGH	LOW	NOMINAL	HIGH	LOW
DC NMH, V	0.15	0.2	0.1	0.1	0.2	0.1
DC NML, V	0.15	0.15	0.2	0.05	0.05	0.1
AC NMH, V	0.15	0.2	0.15	0.2	0.2	0.2
AC NML, V	0.1	0.1	0.1	0.05	0.05	0.05
Tp0, pS	65	68	64	78	84	80
Tp/FO, pS	14	15	12	13	14	11
Tp/fF, pS	2	1.7	2.3	2.1	2	2.2
PD, mW	603	574	665	589	565	615

TABLE 5.2. DCFL WITH FANIN = 3

	T = 25° C			T = 125° C		
	NOMINAL	HIGH	LOW	NOMINAL	HIGH	LOW
DC NMH, V	0.2	0.3	0.15	0.15	0.15	0.1
DC NML, V	0.15	0.1	0.15	0.1	0.1	0.1
AC NMH, V	0.2	0.15	0.2	0.1	0.1	0.1
AC NML, V	0.2	0.15	0.15	0.15	0.1	0.15
Tp0, pS	49	51	44	49	49	46
Tp/FO, pS	5	4	3	6	7	4
Tp/fF, pS	1.5	1.4	1.8	1.6	1.5	1.7
PD, mW	610	580	675	596	572	630

TABLE 5.1. DCFL WITH FANIN = 1

	T = 25° C			T = 125° C		
	NOMINAL	HIGH	LOW	NOMINAL	HIGH	LOW
DC NMH, V	0.15	0.2	0.1	0.1	0.2	0.1
DC NML, V	0.15	0.15	0.2	0.05	0.05	0.1
AC NMH, V	0.15	0.2	0.15	0.2	0.2	0.2
AC NML, V	0.1	0.1	0.1	0.05	0.05	0.05
Tp0, pS	65	68	64	78	84	80
Tp/FO, pS	14	15	12	13	14	11
Tp/fF, pS	2	1.7	2.3	2.1	2	2.2
PD, mW	603	574	665	589	565	615

TABLE 5.2. DCFL WITH FANIN = 3

	T = 25° C			T = 125° C		
	NOMINAL	HIGH	LOW	NOMINAL	HIGH	LOW
DC NMH, V	0.2	0.3	0.15	0.15	0.15	0.1
DC NML, V	0.15	0.1	0.15	0.1	0.1	0.1
AC NMH, V	0.2	0.15	0.2	0.1	0.1	0.1
AC NML, V	0.2	0.15	0.15	0.15	0.1	0.15
Tp0, pS	49	51	44	49	49	46
Tp/FO, pS	5	4	3	6	7	4
Tp/fF, pS	1.5	1.4	1.8	1.6	1.5	1.7
PD, mW	610	580	675	596	572	630

5.4. Source Follower FET Logic (SFL)

A schematic for an SFL 3 input NOR gate is shown in Figure 5.12. The SFL transfer characteristics are shown in Figures 5.13 to 5.16 at 25 and 125° C for nominal, high, and low model with FANIN=1 and 3. Figures 5.17 and 5.18 show the power delay product for this family at 25 and 125° C.

Tables 5.3 and 5.4 summarize the SFL characteristics at 25 and 125° C for FANIN of 1 and 3.

TABLE 5.3. SFL WITH FANIN = 1

	T = 25° C			T = 125° C		
	NOMINAL	HIGH	LOW	NOMINAL	HIGH	LOW
DC NMH, V	0.4	0.5	0.25	0.3	0.4	0.2
DC NML, V	0.55	0.45	0.6	0.4	0.3	0.5
AC NMH, V	0.4	0.4	0.3	0.3	0.3	0.3
AC NML, V	0.5	0.5	0.6	0.4	0.3	0.3
Tp0, pS	100	108	92	107	115	94
Tp/FO, pS	10	11	9	13	13	12
Tp/fF, pS	3.2	3.2	3.2	3.4	3.6	3.4
PD, mW	680	660	686	658	652	656

TABLE 5.4.7 SFL WITH FANIN = 3

	T = 25° C			T = 125° C		
	NOMINAL	HIGH	LOW	NOMINAL	HIGH	LOW
DC NMH, V	0.55	0.6	0.4	0.5	0.55	0.35
DC NML, V	0.45	0.3	0.5	0.2	0.15	0.3
AC NMH, V	0.45	0.4	0.35	0.4	0.4	0.3
AC NML, V	0.45	0.35	0.35	0.3	0.15	0.25
Tp0, pS	70	75	63	85	85	75
Tp/FO, pS	10	10	10	9	10	9
Tp/fF, pS	2.7	2.8	2.6	3	3.1	3
PD, mW	675	671	704	667	660	678

5.5. Push/Pull SFL

A schematic for the push/pull SFL 3 input NOR gate is shown in Figure 5.19. Push/pull SFL transfer characteristics are shown in Figures 5.20 to 5.23 using nominal, high, and low current models for FANIN=1 and 3. The power delay characteristics are shown in Figures 5.24 and 5.25.

The summary of Push/Pull SFL characteristics are shown in Tables 5.5 and 5.6.

TABLE 5.5. PUSH/PULL SFL WITH FANIN = 1

	T = 25° C			T = 125° C		
	NOMINAL	HIGH	LOW	NOMINAL	HIGH	LOW
DC NMH, V	0.3	0.4	0.2	0.2	0.3	0.15
DC NML, V	0.35	0.3	0.4	0.3	0.15	0.35
AC NMH, V	0.4	0.35	0.35	0.25	0.25	0.25
AC NML, V	0.35	0.35	0.3	0.25	0.3	0.2
Tp0, pS	74	73	74	76	77	75
Tp/FO, pS	9	8	9	8.5	7	9
Tp/fF, pS	2	1.7	2.3	2.1	1.9	2.2
PD, mW	666	677	624	676	725	656

TABLE 5.6. PUSH/PULL SFL WITH FANIN = 3

	T = 25° C			T = 125° C		
	NOMINAL	HIGH	LOW	NOMINAL	HIGH	LOW
DC NMH, V	0.3	0.4	0.3	0.3	0.3	0.2
DC NML, V	0.35	0.2	0.4	0.2	0.1	0.3
AC NMH, V	0.4	0.35	0.35	0.25	0.25	0.25
AC NML, V	0.4	0.4	0.4	0.3	0.3	0.3
Tp0, pS	65	66	73	72	70	74
Tp/FO, pS	4	3	5	4.5	4	6.5
Tp/fF, pS	1.5	1.35	1.8	1.6	1.5	1.7
PD, mW	674	689	637	688	745	670

5.6. FET Injection Logic (FIL)

A schematic for a FIL 3 input/3 output NAND gate is shown in Figure 5.26. The FIL DC transfer characteristics are insensitive to FANIN or FANOUT due to the open drain output of the gate as will be shown. The DC transfer characteristics for nominal, high, and low current models are shown in Figures 5.27 to 5.30 at 25 and 125° C. Power delay product for FIL are shown in Figures 5.31 and 5.32.

The FIL characteristics are summarized in Tables 5.7 and 5.8.

TABLE 5.7. FIL WITH FANIN = 3, FANOUT = 1

	T = 25° C			T = 125° C		
	NOMINAL	HIGH	LOW	NOMINAL	HIGH	LOW
DC NMH, V	0.2	0.2	0.1	0.1	0.1	0.05
DC NML, V	0.65	0.55	0.7	0.5	0.4	0.6
AC NMH, V	0.4	0.4	0.35	0.35	0.35	0.35
AC NML, V	0.6	0.6	0.6	0.5	0.5	0.5
Tp0, pS	50	53	49	49	49	50
Tp/FO, pS	16	16	15	14	15	13
Tp/fF, pS	2.8	2.8	2.7	2.4	2.5	2.4
PD, mW	571	531	593	535	512	562

TABLE 5.8. FIL WITH FANIN = 3, FANOUT = 3

	T = 25° C			T = 125° C		
	NOMINAL	HIGH	LOW	NOMINAL	HIGH	LOW
DC NMH, V	0.15	0.15	0.05	0.1	0.1	0.05
DC NML, V	0.7	0.6	0.7	0.5	0.5	0.6
AC NMH, V	0.4	0.4	0.3	0.3	0.3	0.3
AC NML, V	0.6	0.6	0.6	0.5	0.5	0.5
Tp0, pS	97	101	94	92	95	89
Tp/FO, pS	16	16	15	14	15	13
Tp/fF, pS	2.6	2.7	2.5	2.2	2.4	2.1
PD, mW	579	541	606	543	521	576

5.7. Comparative Analysis

Analysis of the data shows that, as expected, DCFL has the shortest propagation delay. It was also expected that DCFL will have the smallest noise margins, which is more pronounced at high temperature and prevents the implementation of complex gates. However, DCFL has a number of attractive features namely, high speed, simplicity, low power, and current steering due to Schottky diode conduction when the input is high. Given present GaAs technology, DCFL is most suitable in implementing very high speed, small scale circuits where the threshold voltage variations are easily controlled. This family at present is not suitable for LSI density circuits unless the threshold voltage variation is repeatably controlled to below 25 mV. The DCFL logic family can greatly benefit if a number of device improvements are incorporated. The improvements are increasing the output resistance and transconductance of GaAs FETs, however, the greatest improvement is realized if the Schottky barrier height is increased to about 1.0 volt.

The data shows that the Source Follower logic family is robust and has noise margins 3 times higher than DCFL. However, this family is about twice as slow as DCFL. This is to be expected since there are two stages from input to output. Also the SFL family dissipates slightly more power, and requires more transistor count to implement a NOR gate. The data indicates that SFL is capable of implementing LSI

density circuits with a penalty of increased chip area and decrease of circuit performance. However, the ability to implement complex gates in SFL can result in reducing the gate count compared to DCFL. Hence, use of SFL can result in reduced chip area and power dissipation, and increased chip performance. However, circuit performance can be close to DCFL when designing high fanout circuits due to the low input capacitance of the SFL gate.

The push/pull SFL logic family is also robust and has twice the noise margins of DCFL. This family can achieve DCFL performance especially with high fanouts. The SFL families have the inherent advantage of low input capacitance and do not suffer from the Miller capacitance effect as much as DCFL. The data shows that push/pull SFL can implement very high speed LSI density circuits. The transistor count is certainly higher than DCFL, however, the use of complex gates can greatly reduce the gate count and result in further improvements of reducing power dissipation, propagation delay, and chip area.

The FIL logic family is robust with high AC noise margins 3 times higher than DCFL. This family has an advantage over DCFL and SFL families of being a true current steering logic family. Current steering is very important in the design of high speed GaAs integrated circuits, especially when dealing with small AC noise margins where current transients are high. However, FIL is not as suitable for

implementing very high speed circuits due to the high fanout sensitivity. The ability to implement complex gates in FIL will definitely increase chip performance, however, the delay incurred can be high for fanouts greater than 4. Like the SFL logic families, FIL also requires a higher transistor count per gate when compared to DCFL. But, the power dissipation of FIL is comparable to that of DCFL. This family is most suitable for LSI and VLSI density circuits where the speed of operation is not very important. It can also be used in implementing the slower sections of circuits designed with the above logic families to reduce power dissipation and power supply current transients. The family can be very suitable for designing military circuits where the temperature variations are high, due to FIL's high AC noise margins. This family is also suitable for implementing circuits where RFI coupling and power supply current transients cannot be tolerated, since FIL is truly current steering.

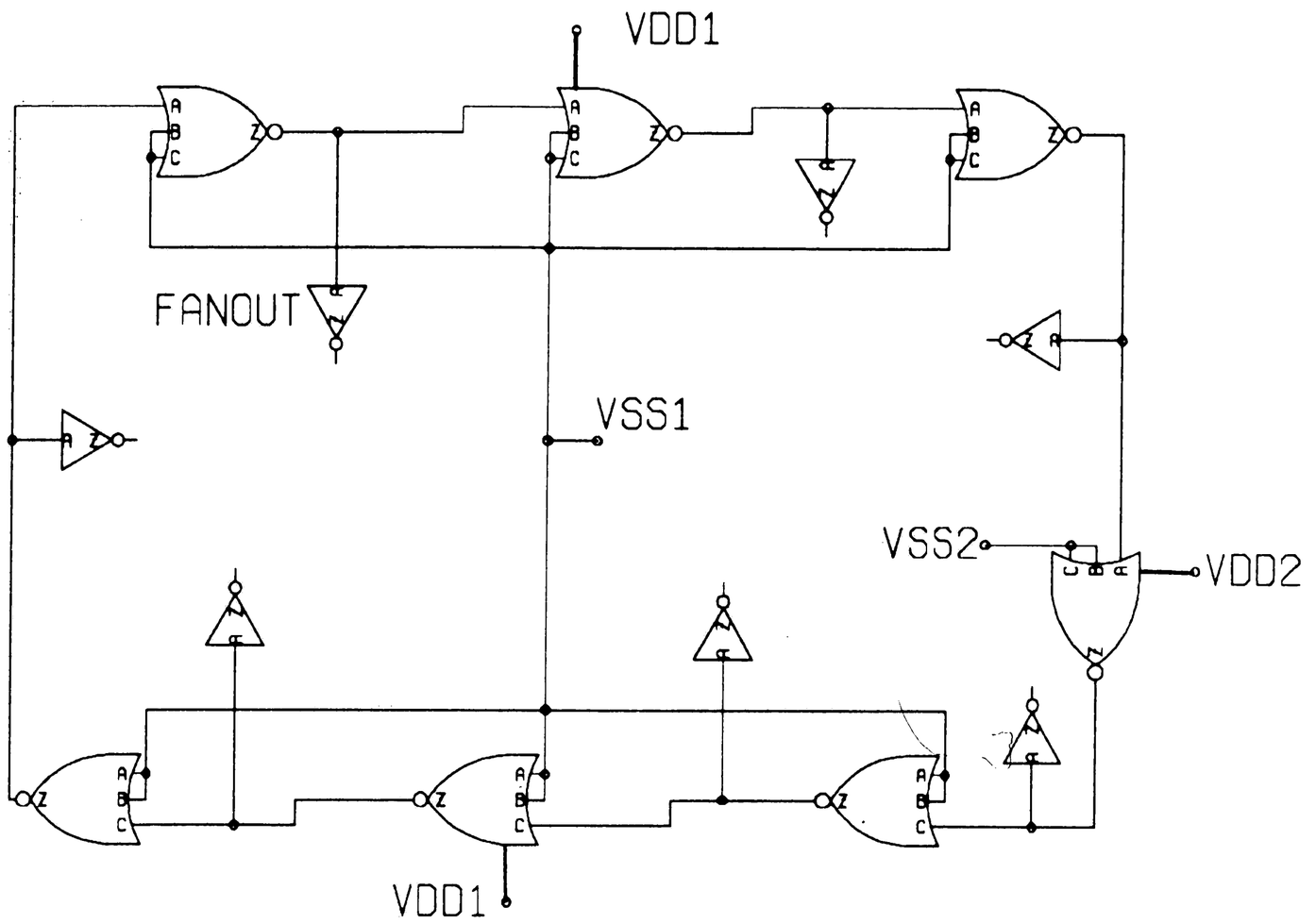


Figure 5.1. Schematic for FANIN=1/FANOUT test.

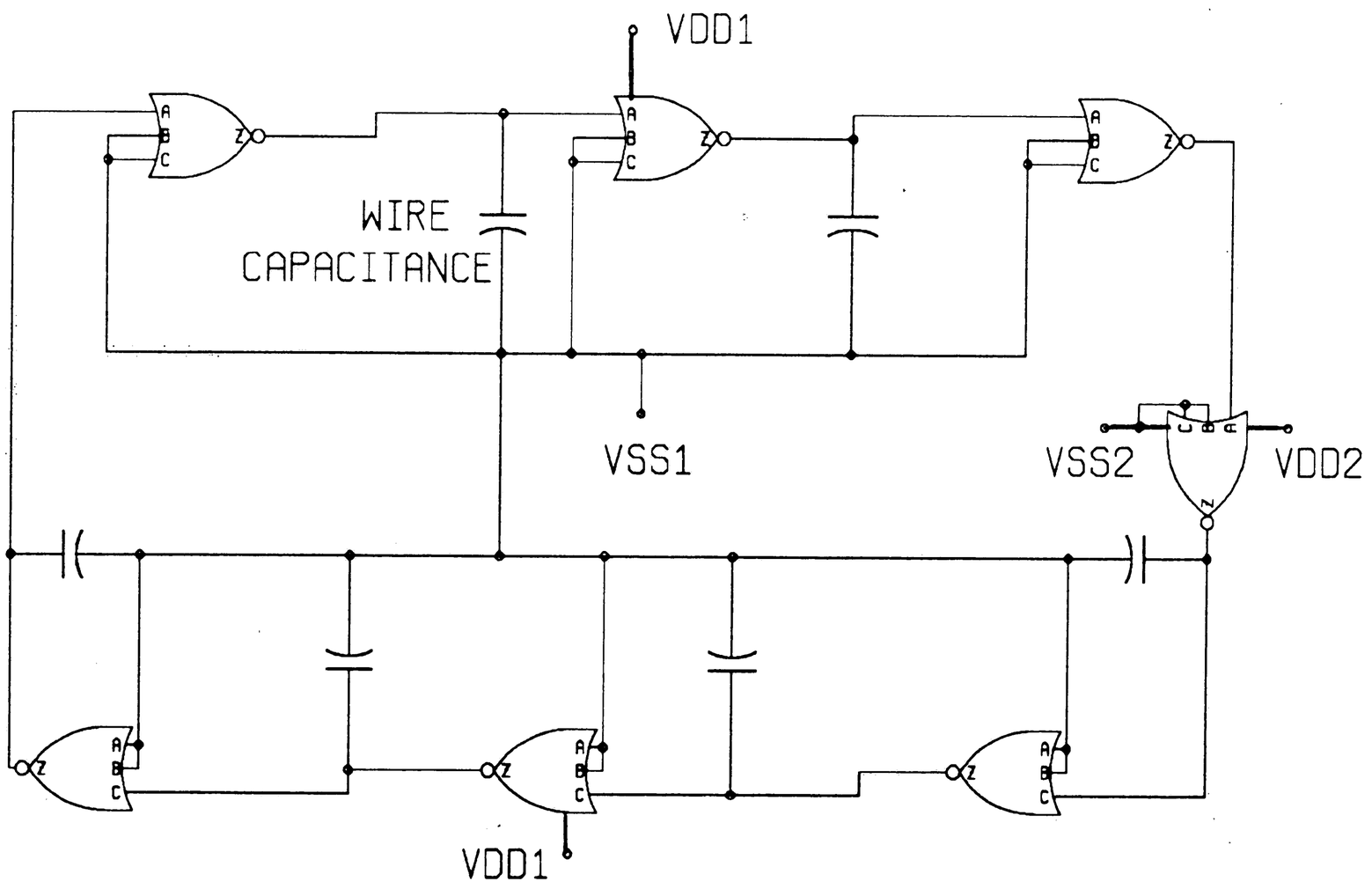


Figure 5.2. Schematic for FANIN=1/wire capacitance test.

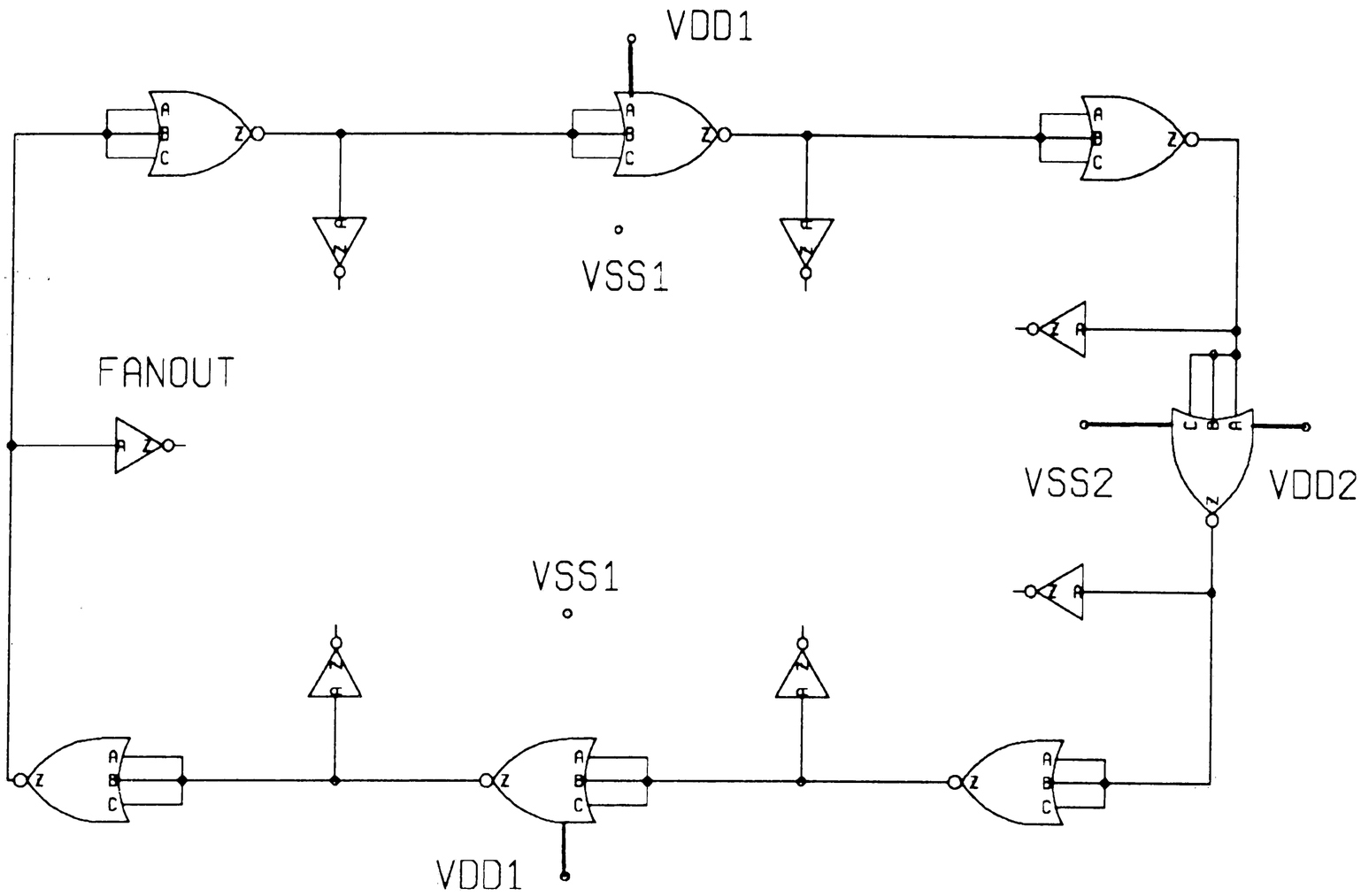


Figure 5.3. Schematic for FANIN=3/FANOUT test.

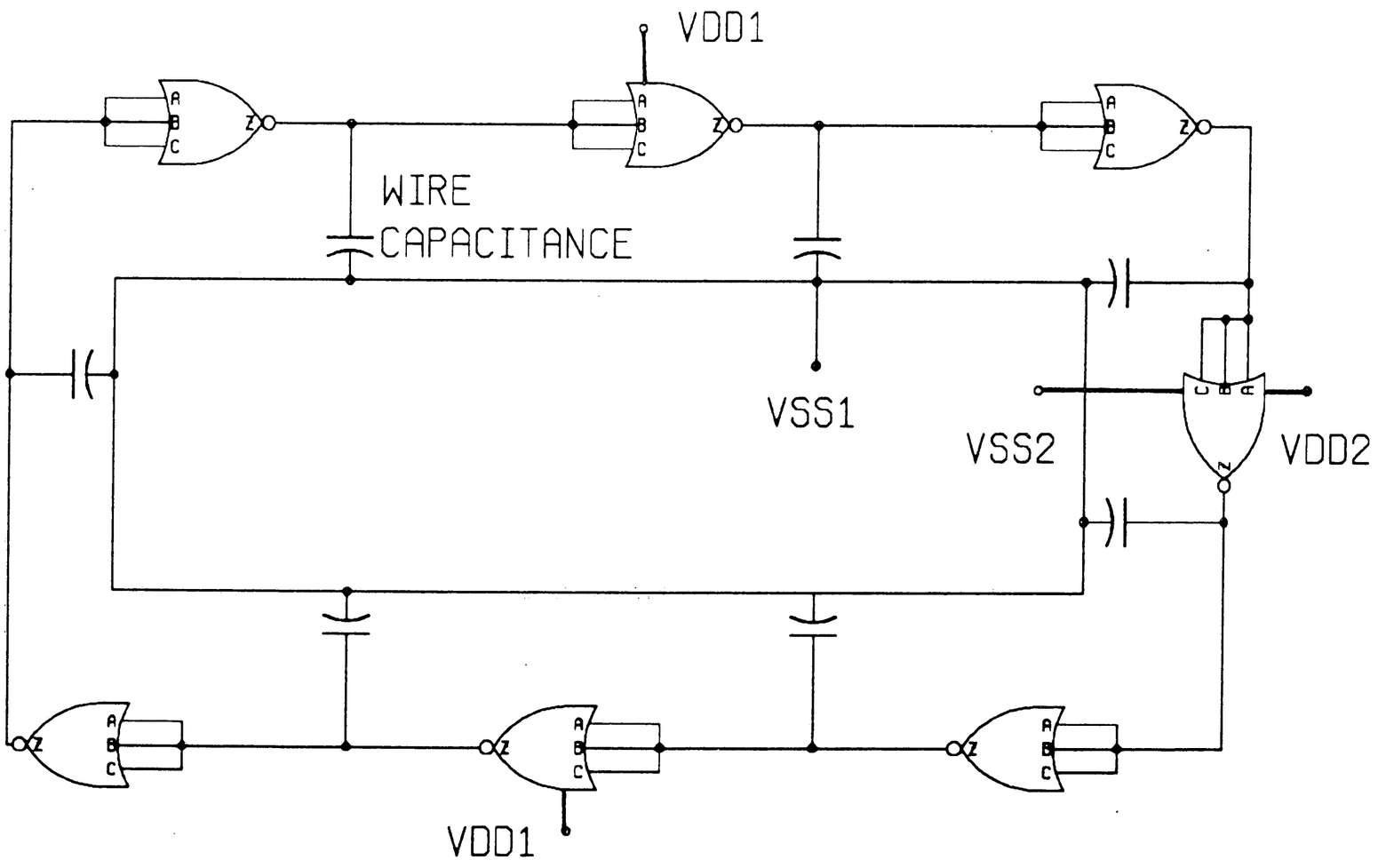


Figure 5.4. Schematic for FANIN=3/wire capacitance test.

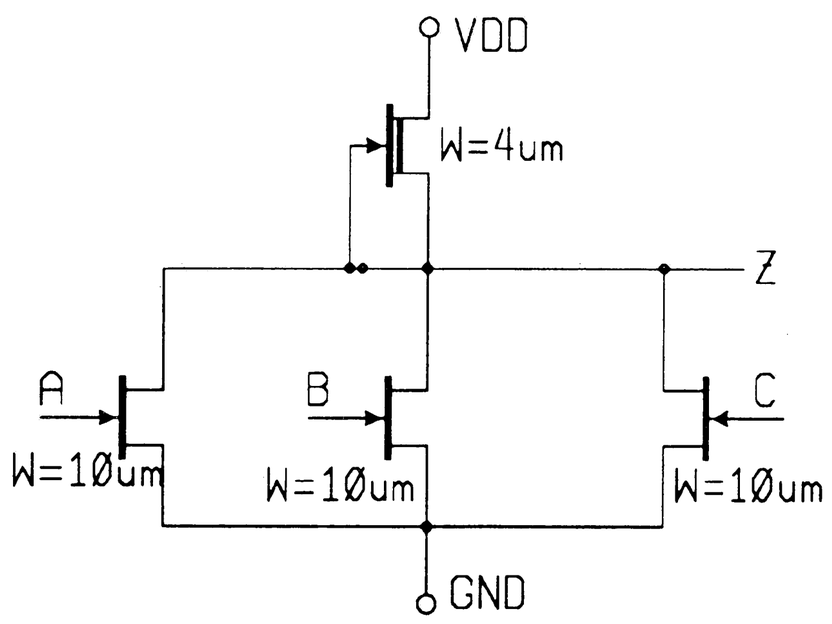


Figure 5.5. DCFL 3 input NOR gate.

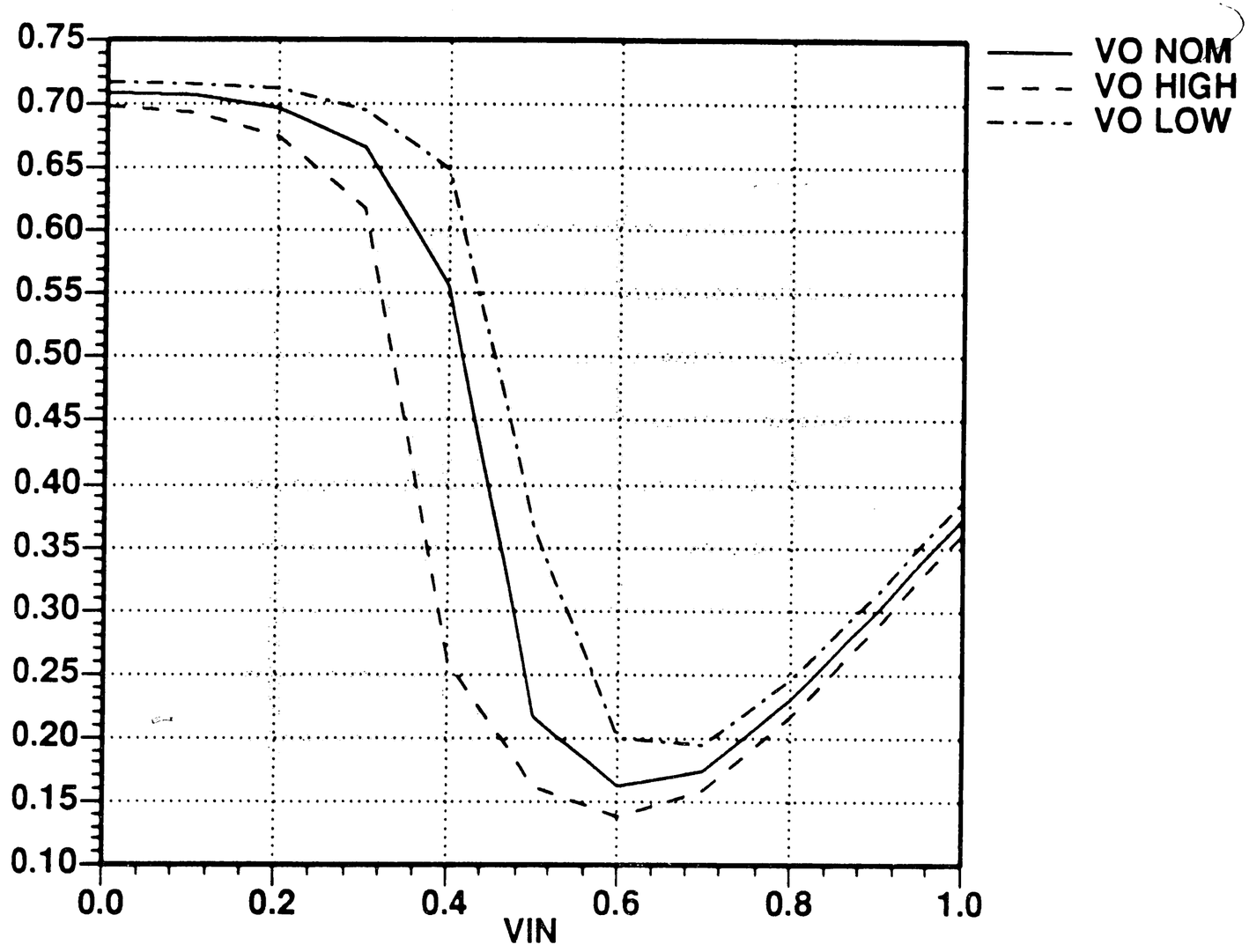


Figure 5.6. DCFL transfer curve, FANIN = 1 at 25° C.

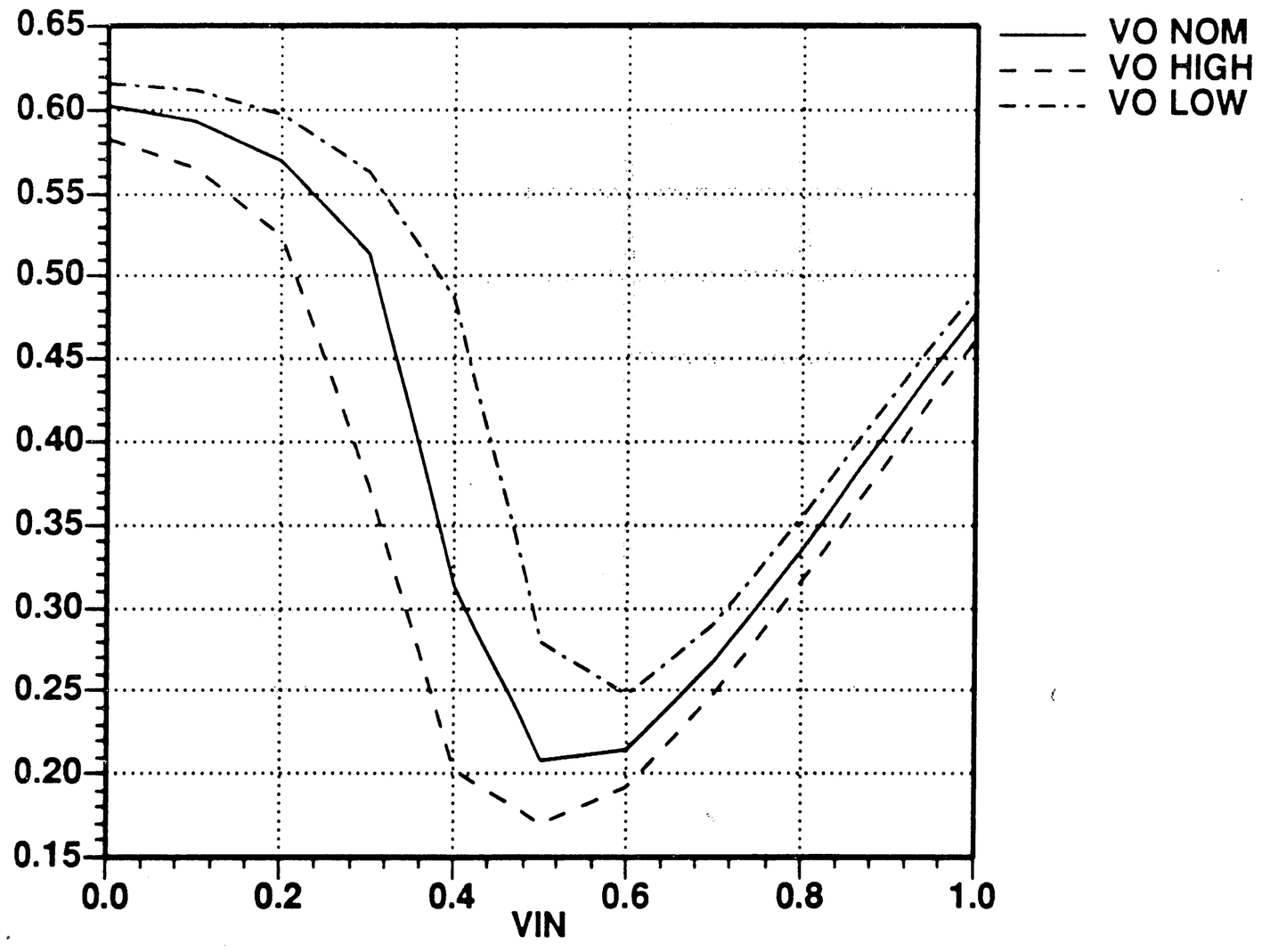


Figure 5.7. DCFL transfer curve, FANIN = 1 at 125° C.

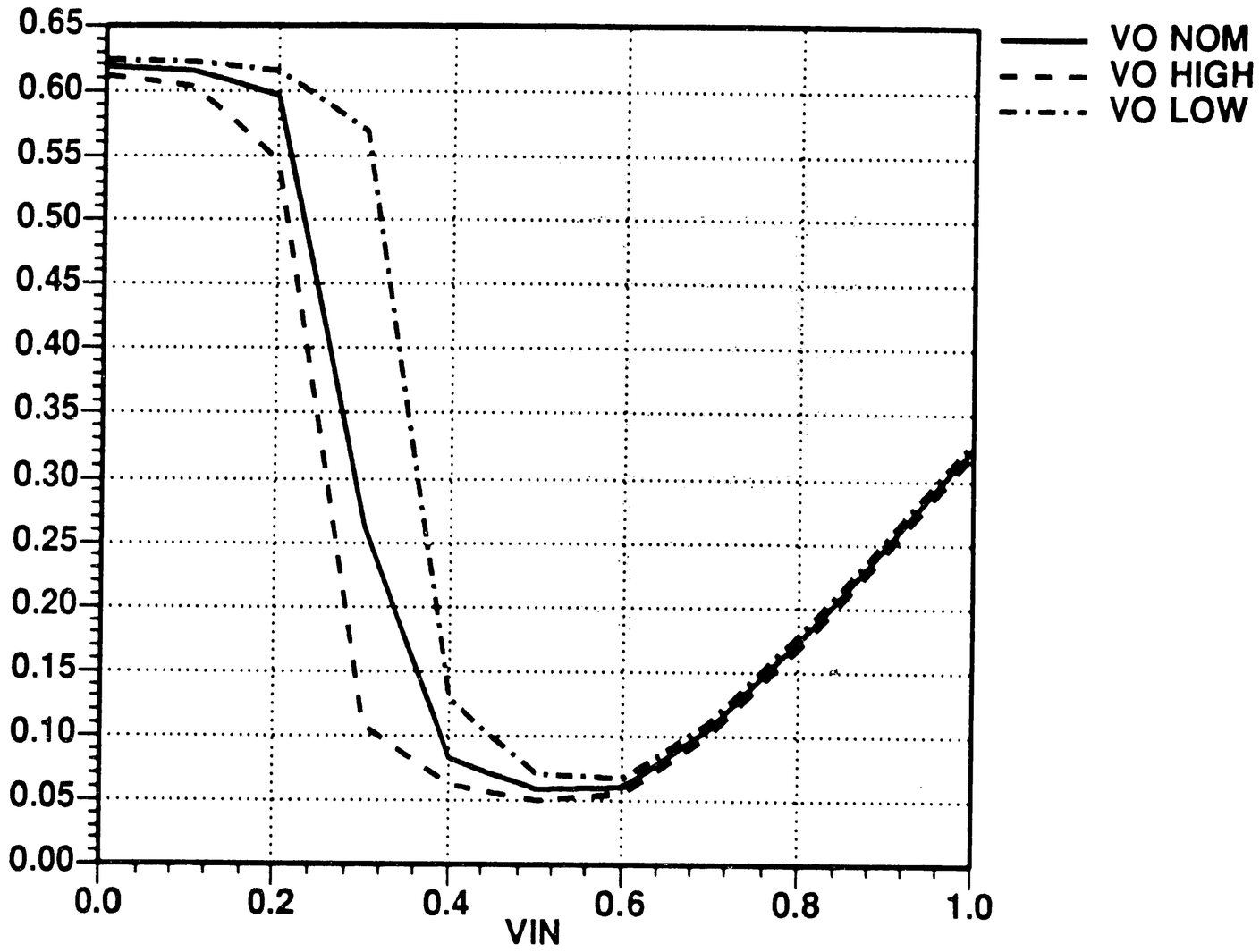


Figure 5.8. DCFL transfer curve, FANIN = 3 at 25° C.

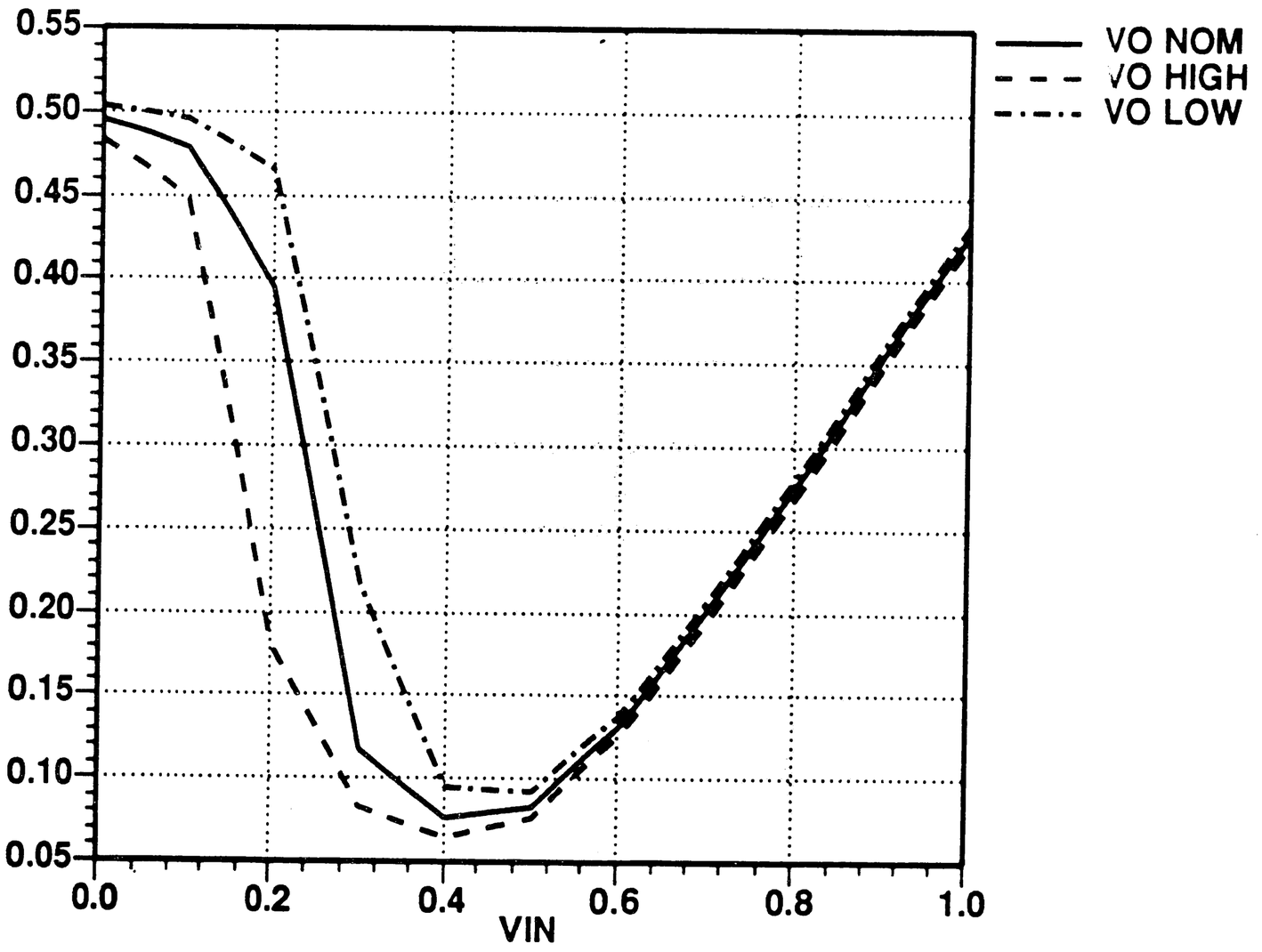


Figure 5.9. DCFL transfer curve, FANIN = 3 at 125° C.

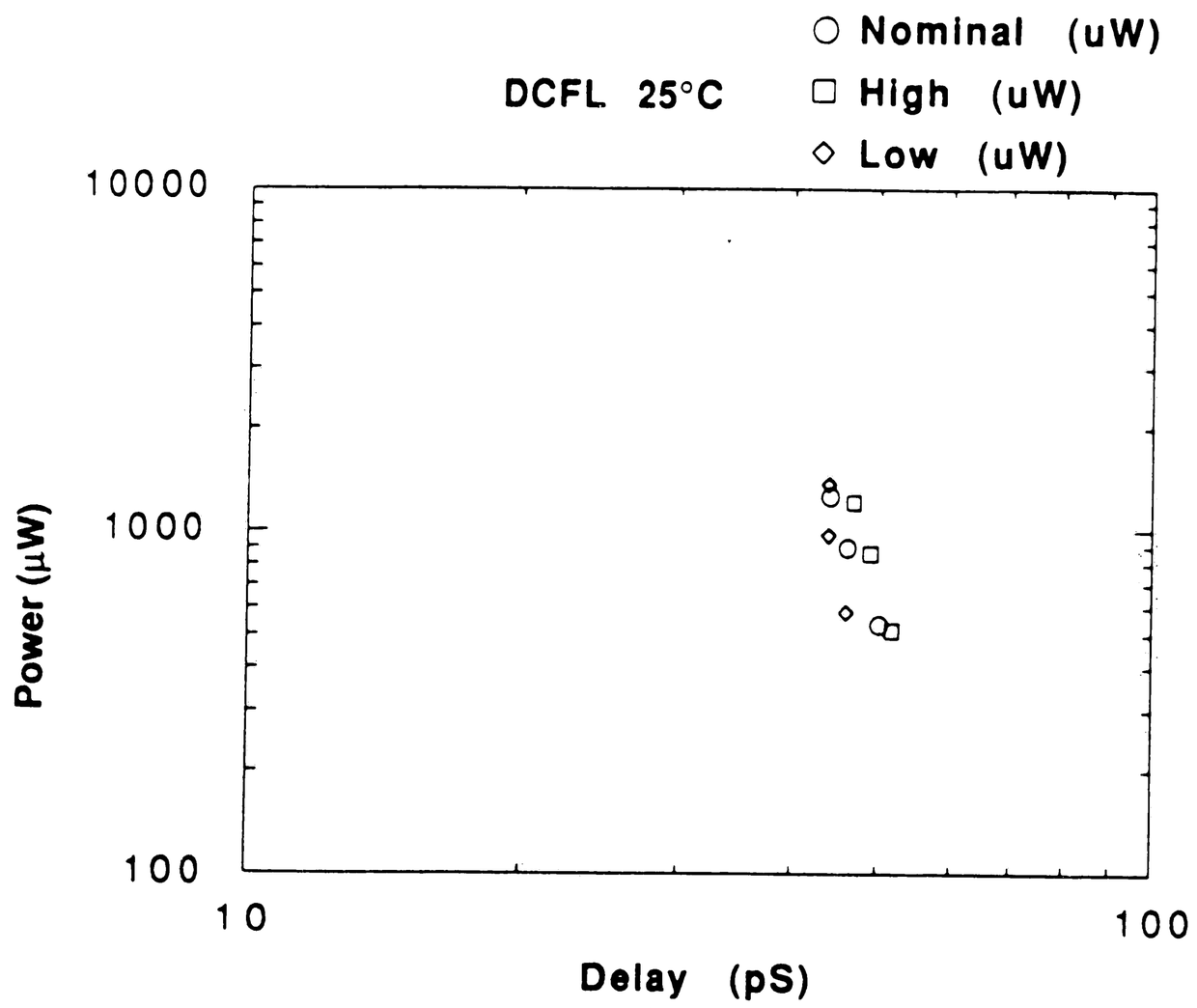


Figure 5.10. DCFL power delay product at 25° C.

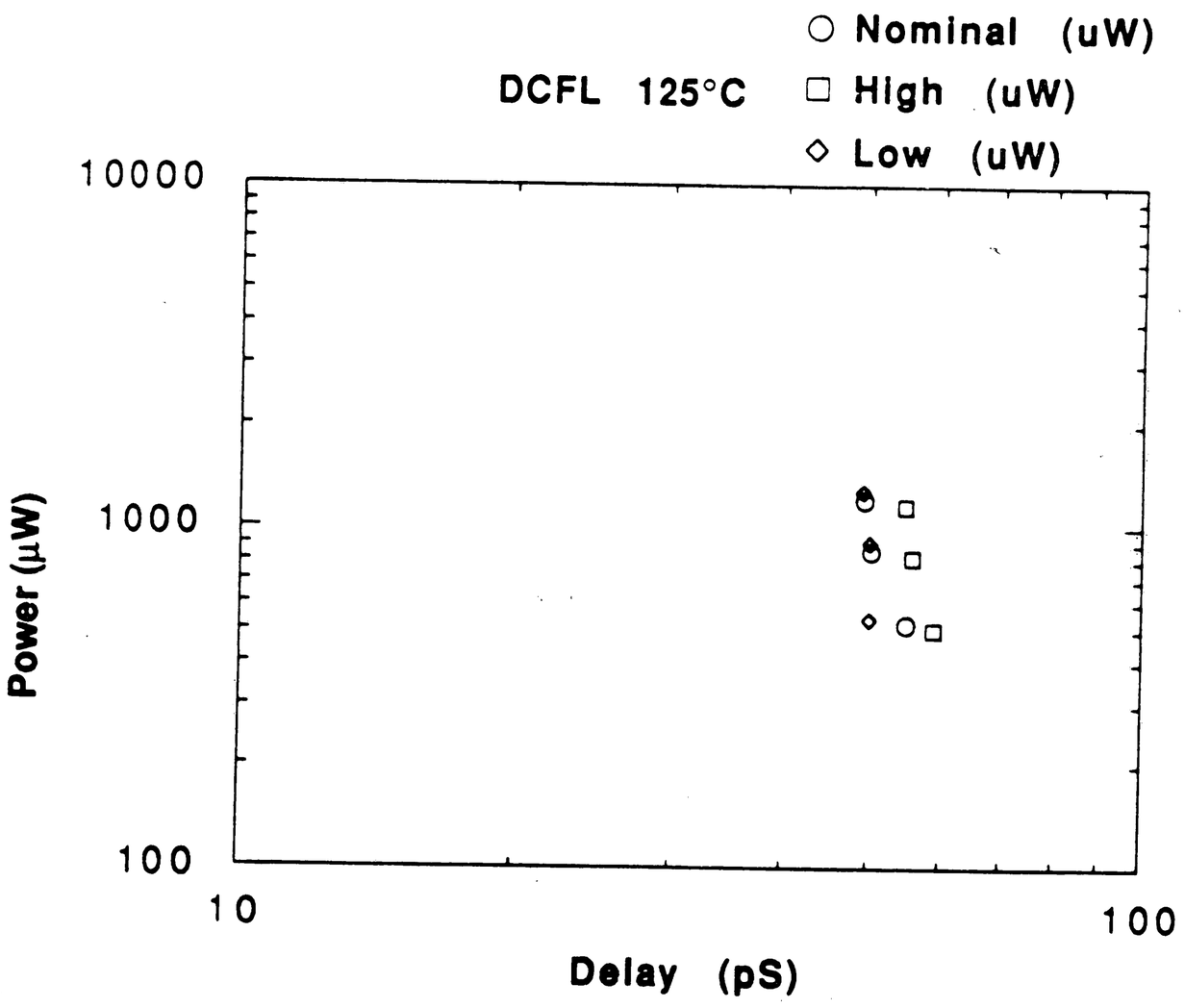


Figure 5.11. DCFL power delay product at 125° C.

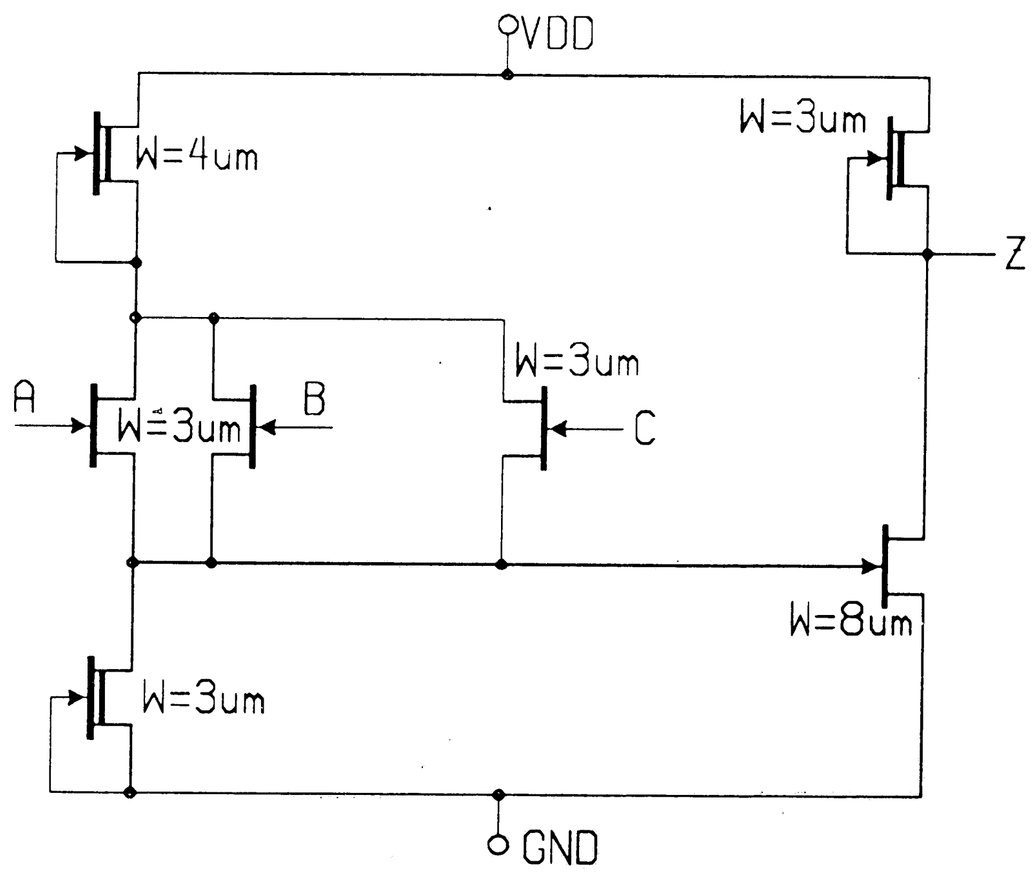


Figure 5.12. SFL 3-input NOR gate.

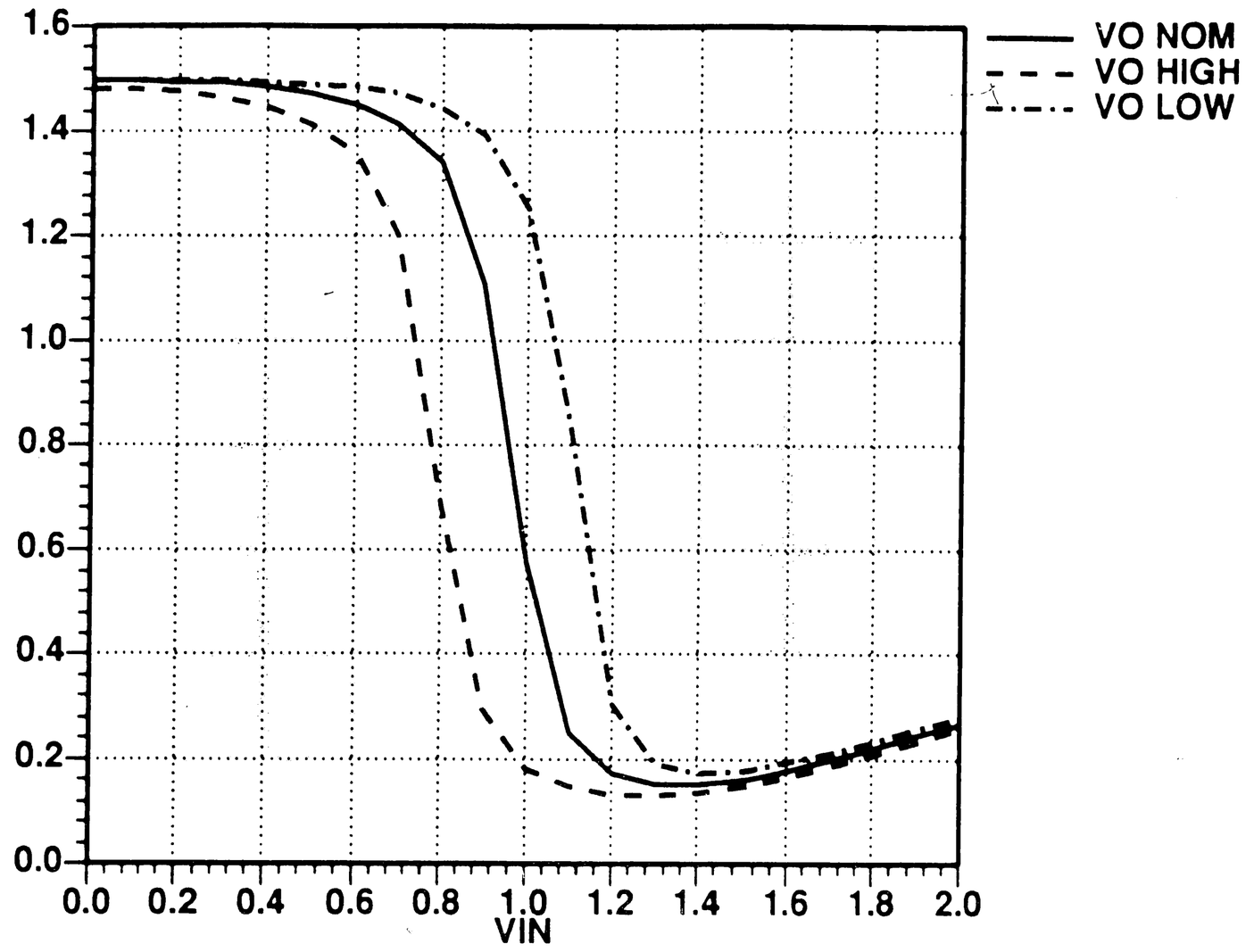


Figure 5.13. SFL transfer curve, FANIN = 1 at 25° C.

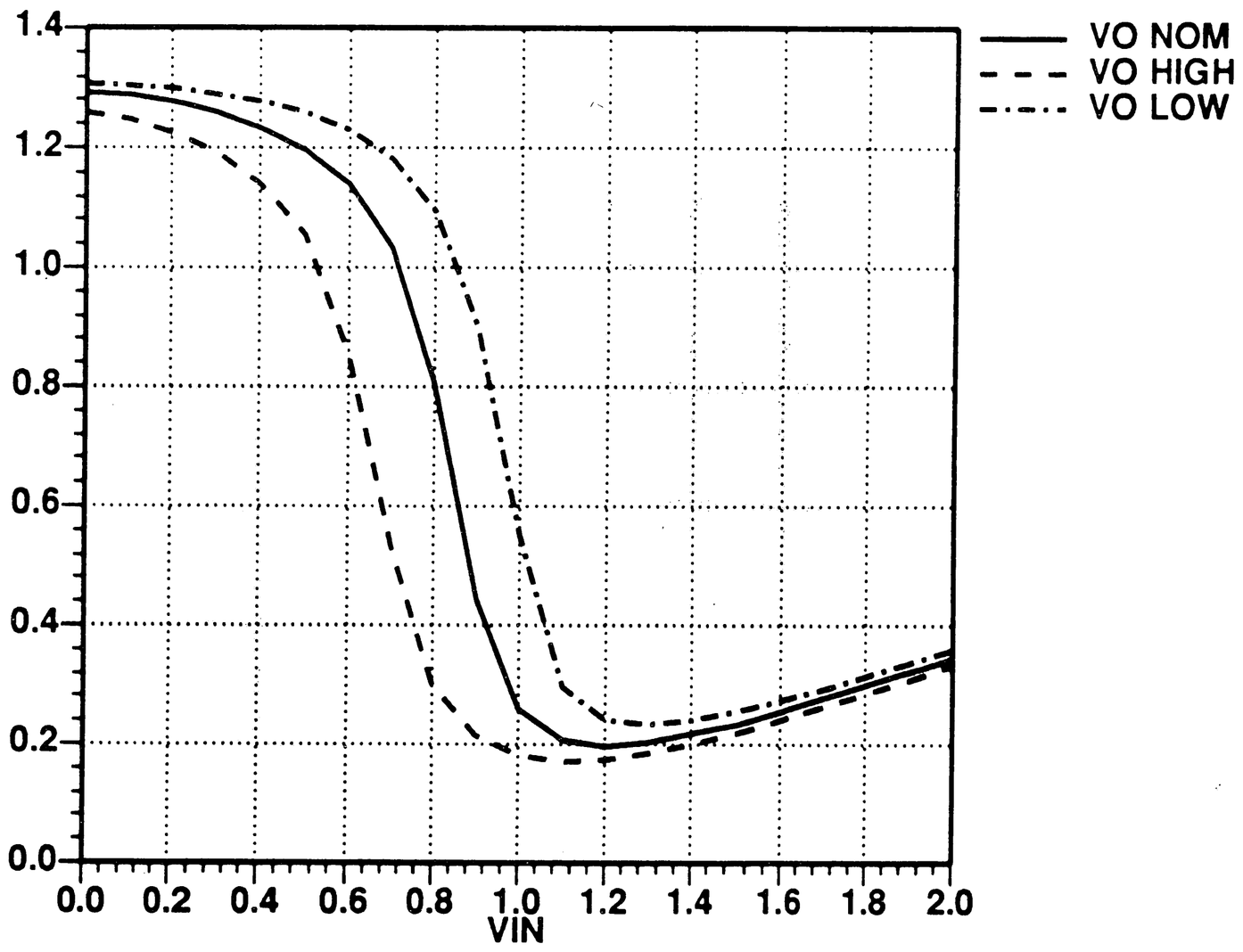


Figure 5.14. SFL transfer curve, FANIN = 1 at 125° C.

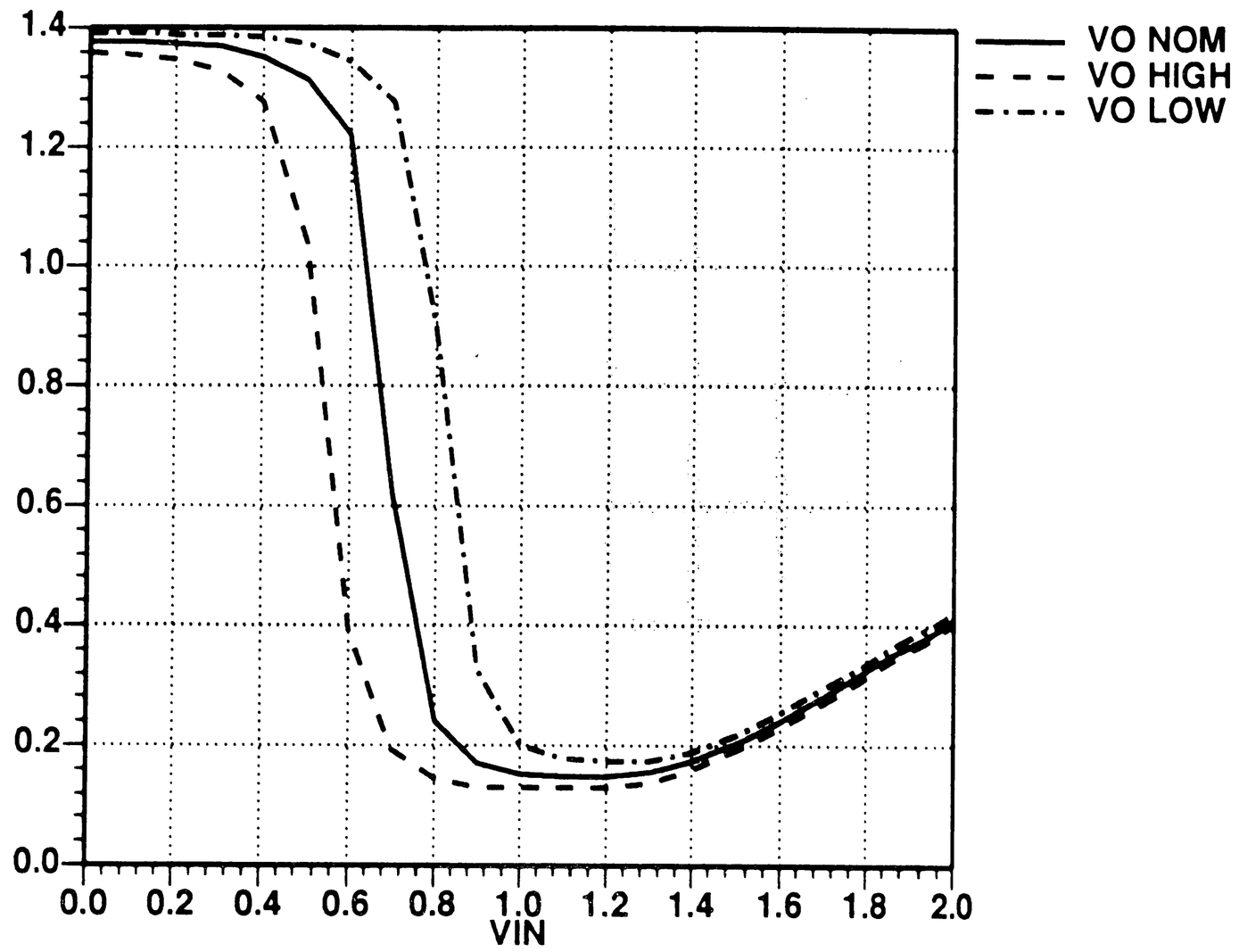


Figure 5.15. SFL transfer curve, FANIN = 3 at 25° C.

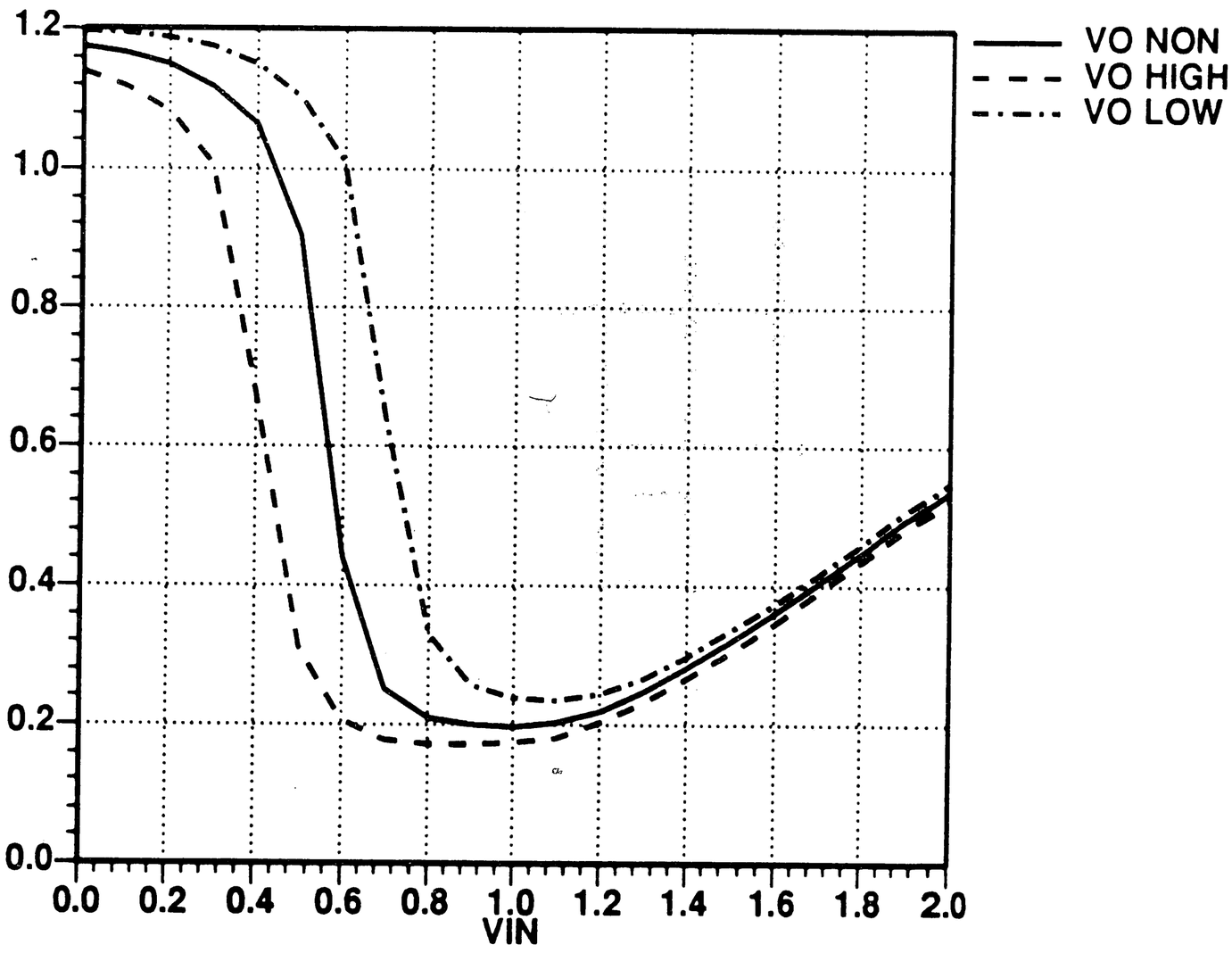


Figure 5.16. SFL transfer curve, FANIN = 3 at 125° C.

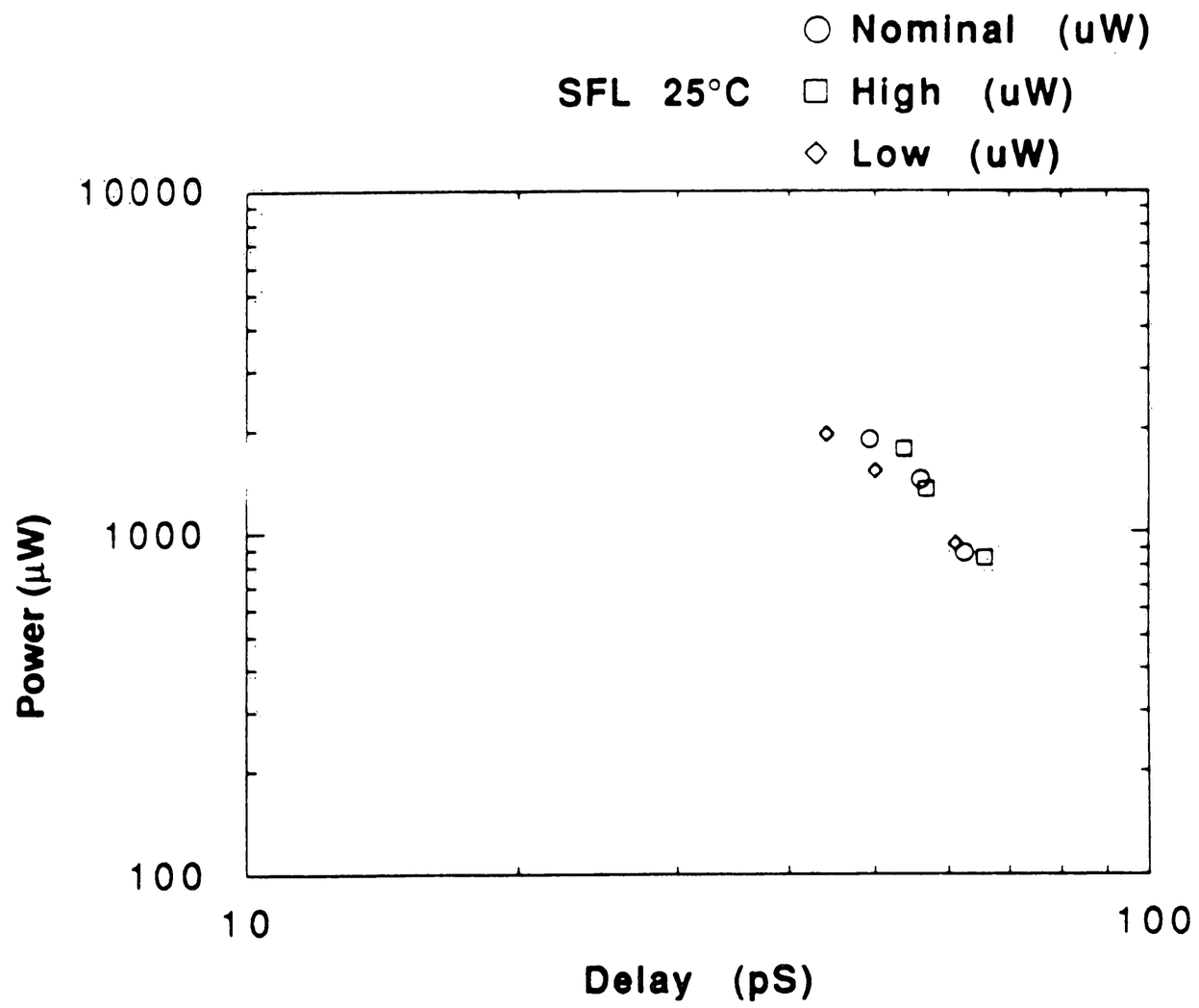


Figure 5.17. SFL power delay product at 25° C.

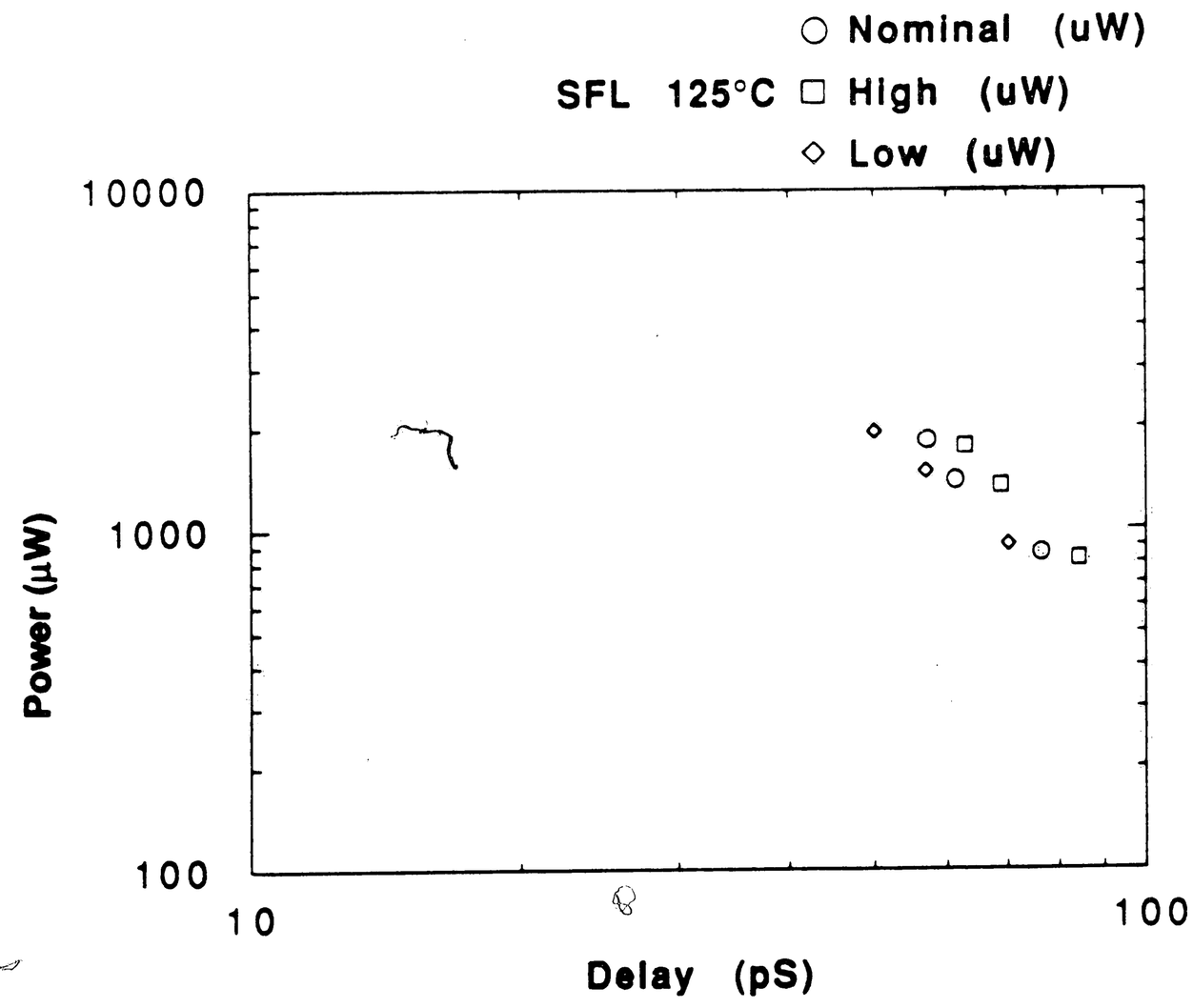


Figure 5.18. SFL power delay product at 125° C.

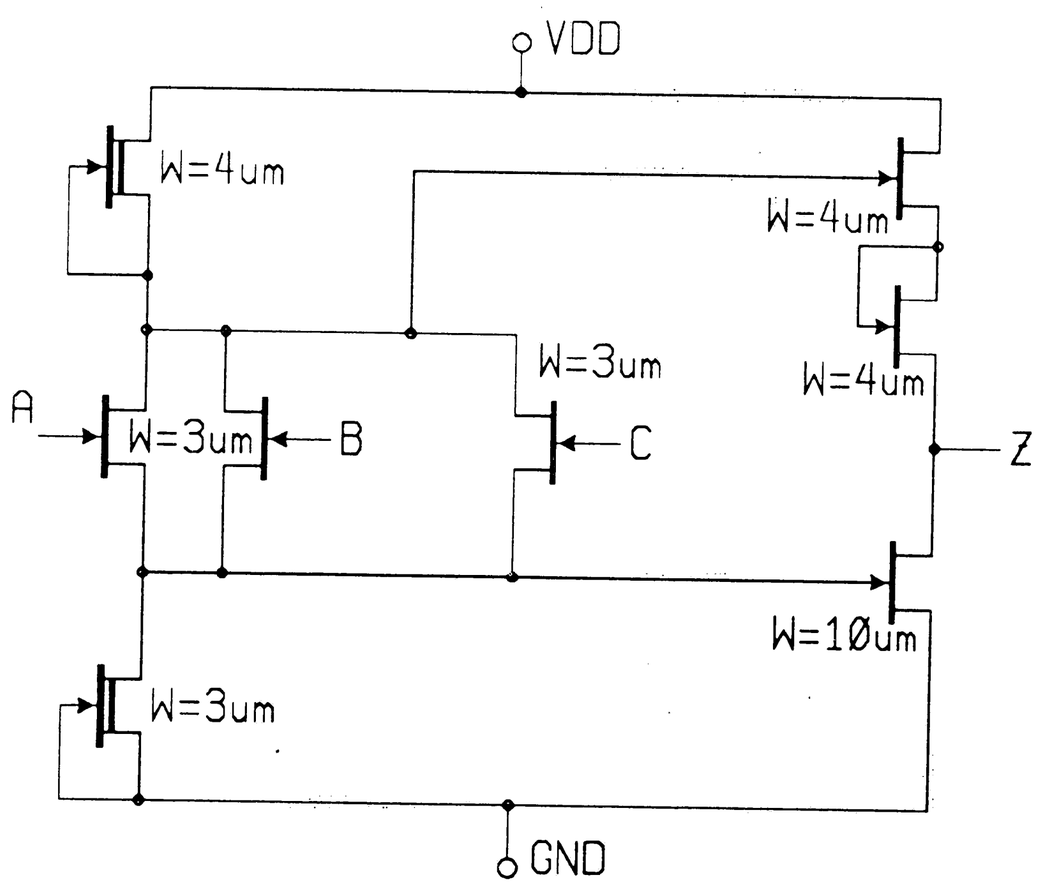


Figure 5.19. Push/Pull SFL 3 input NOR gate.

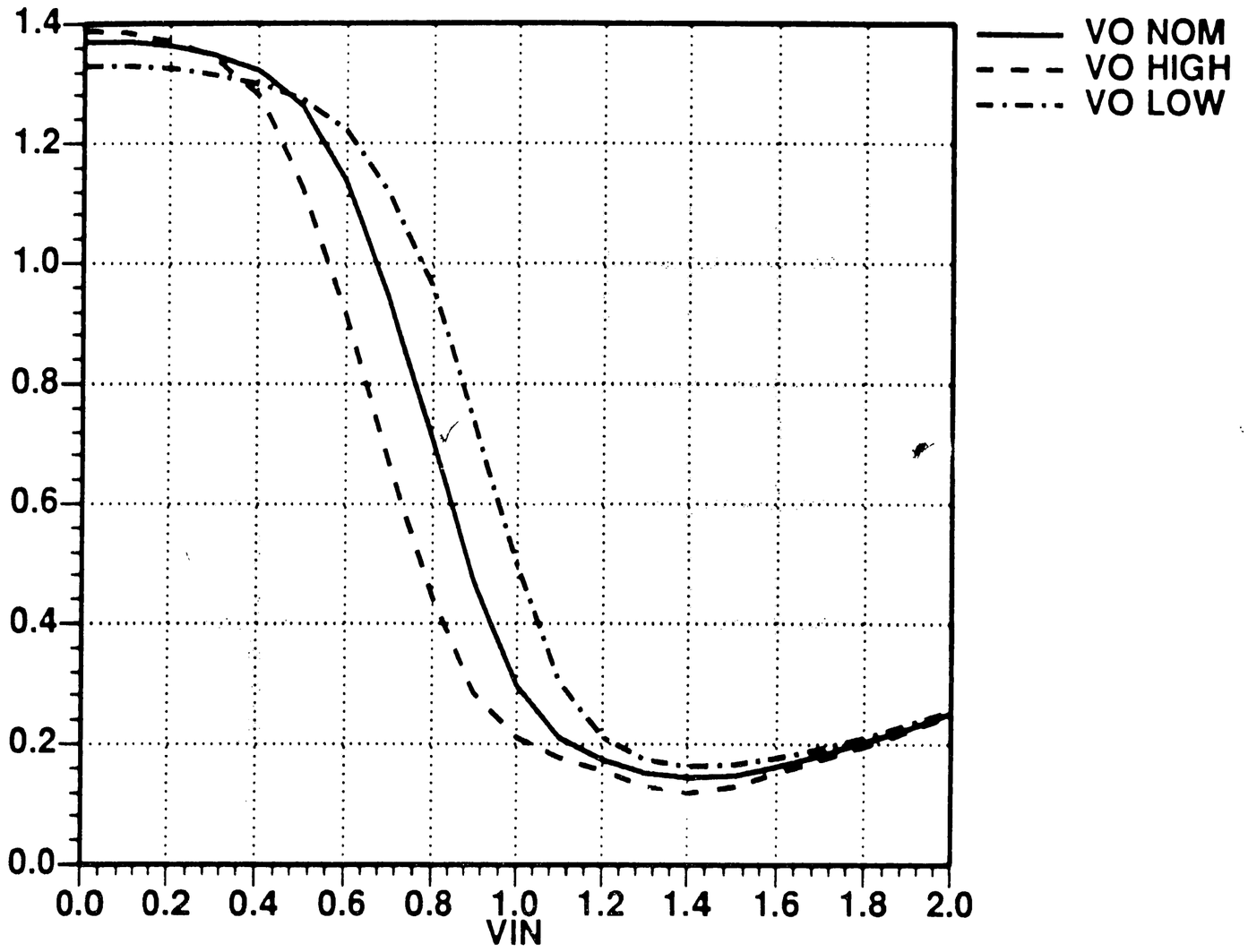


Figure 5.20. Push/Pull SFL transfer curve, fANIN = 1 at 25° C.

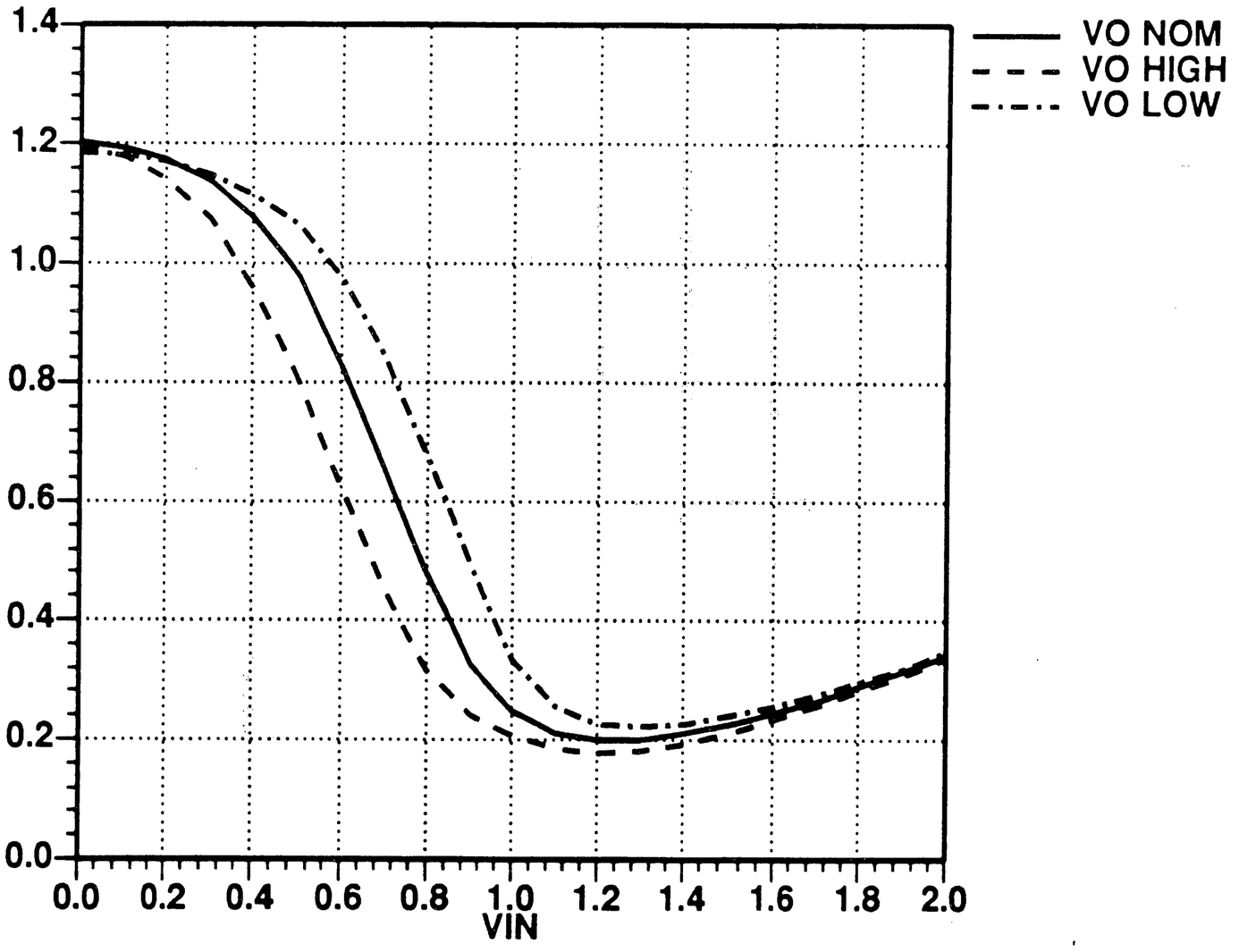


Figure 5.21. Push/Pull SFL transfer curve, FANIN = 1 at 125° C.

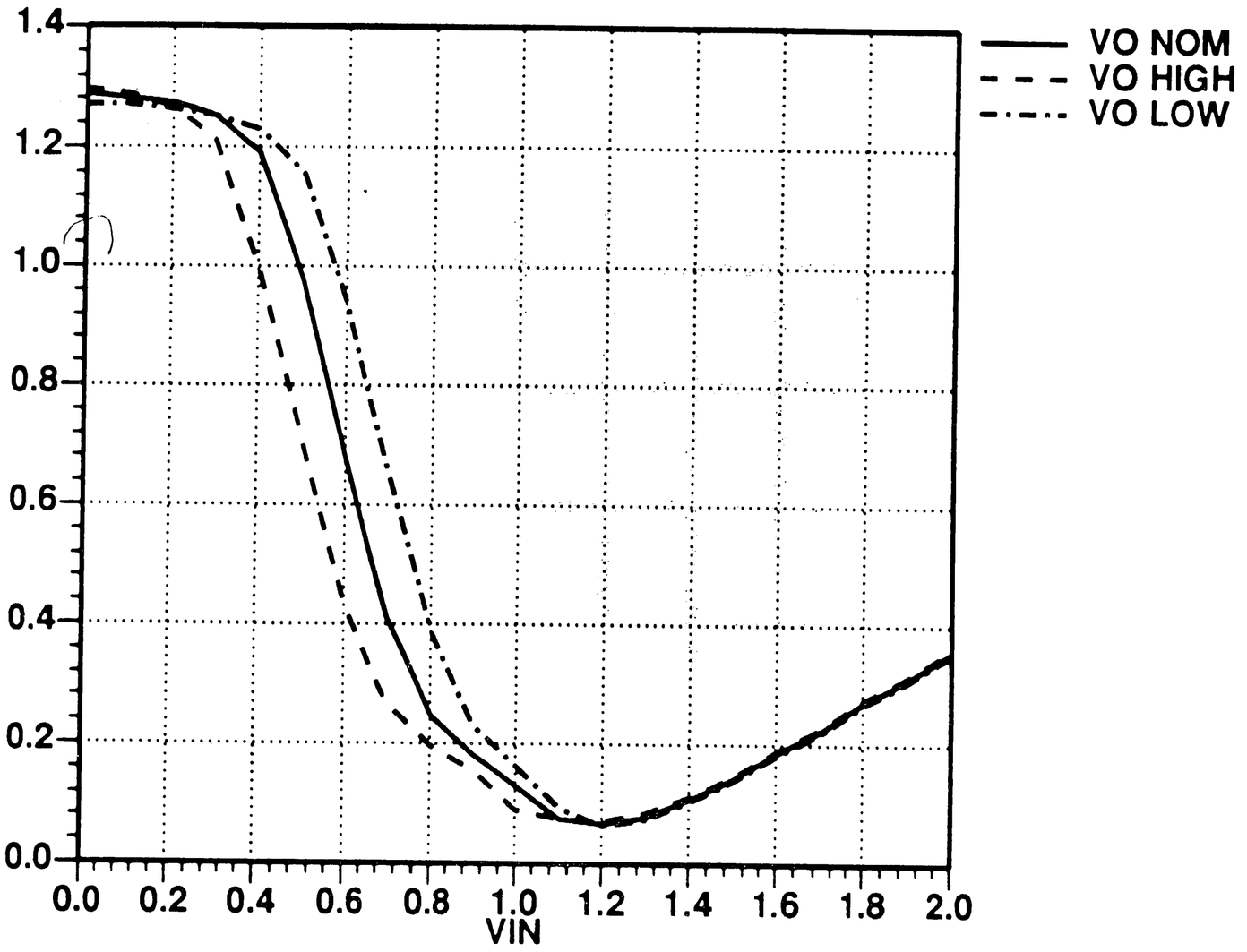


Figure 5.22. Push/Pull SFL transfer curve, FANIN = 3 at 25° C.

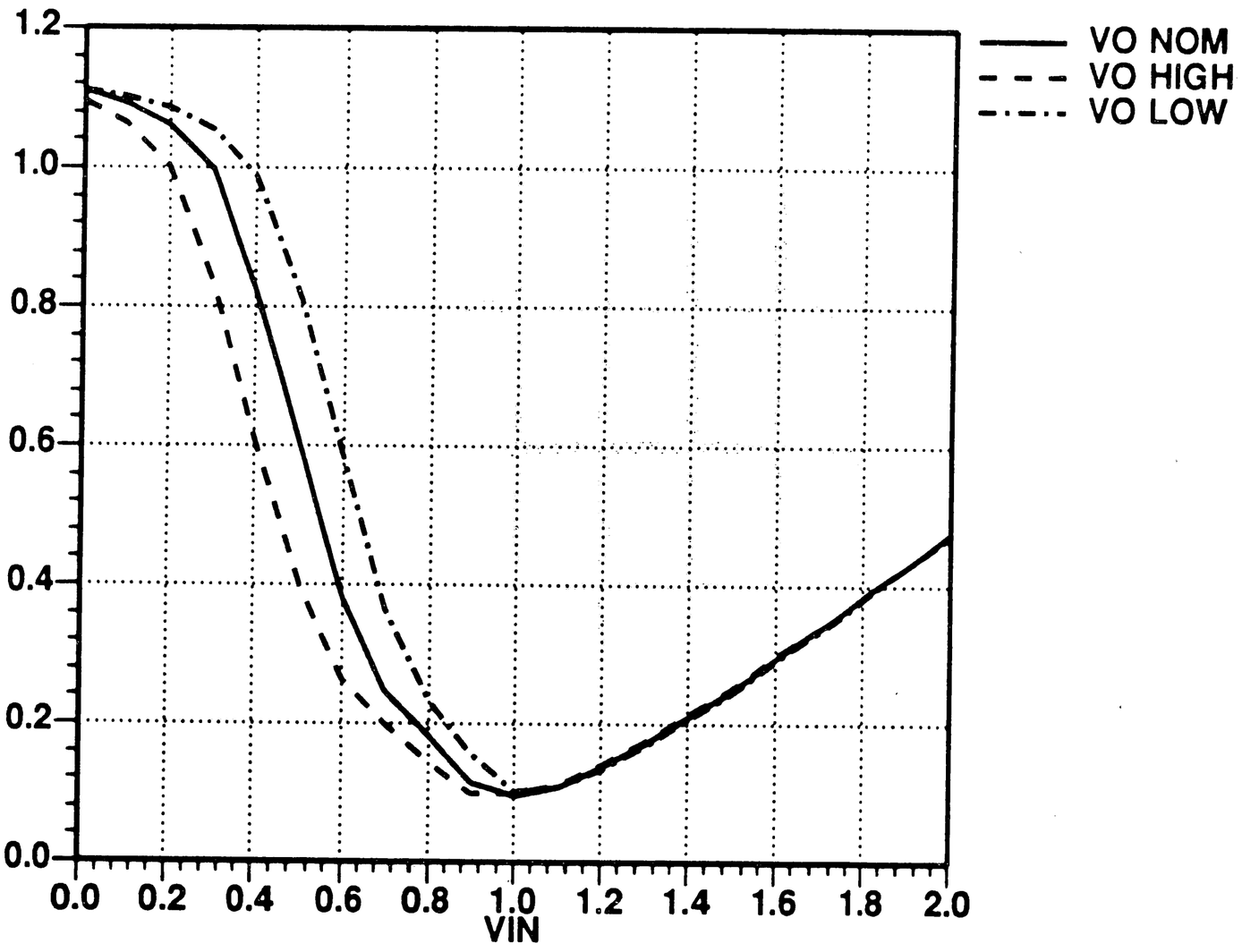


Figure 5.23. Push/Pull SFL transfer curve, FANIN = 3 at 125° C.

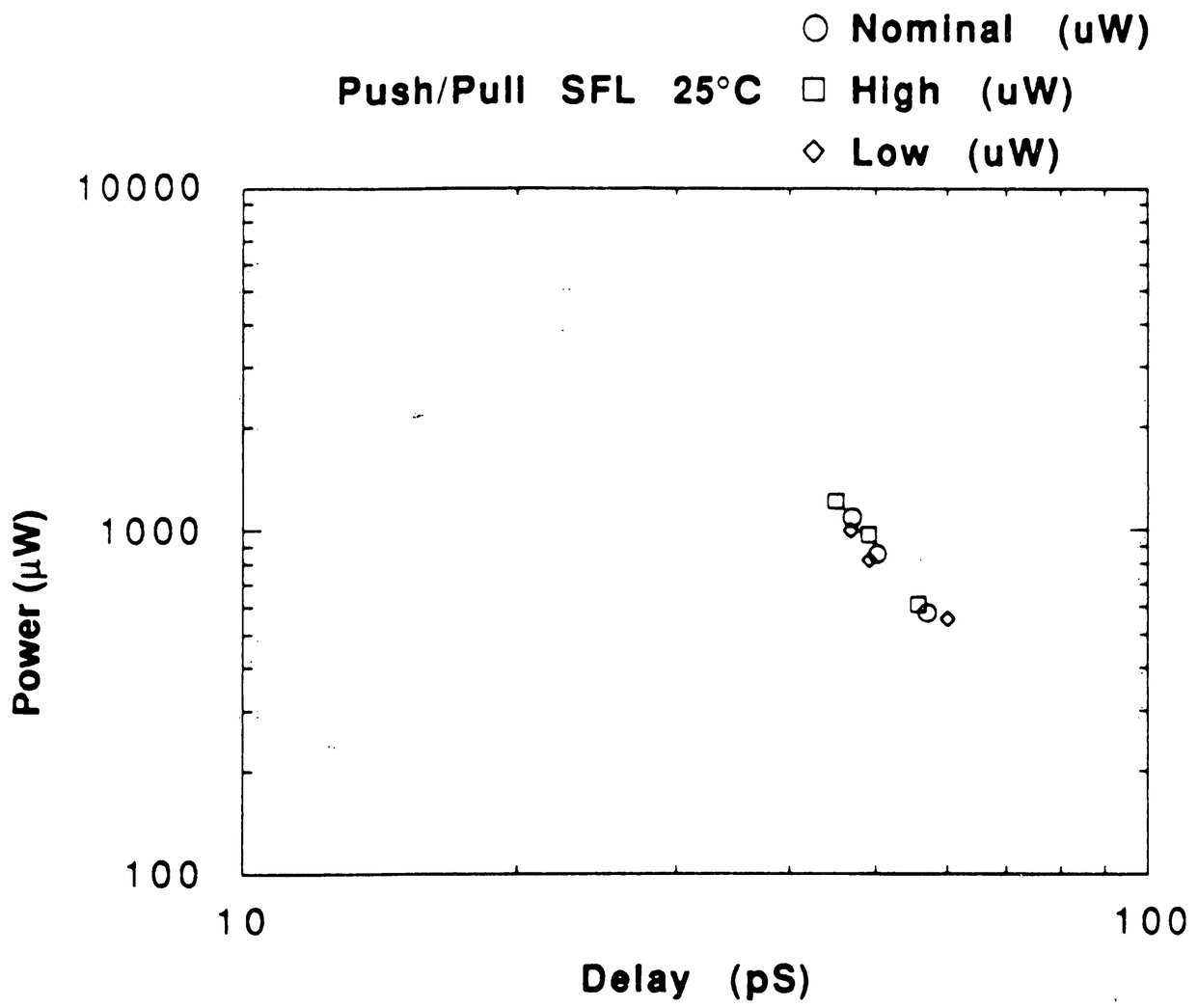


Figure 5.24. Push/Pull SFL power delay product at 25° C.

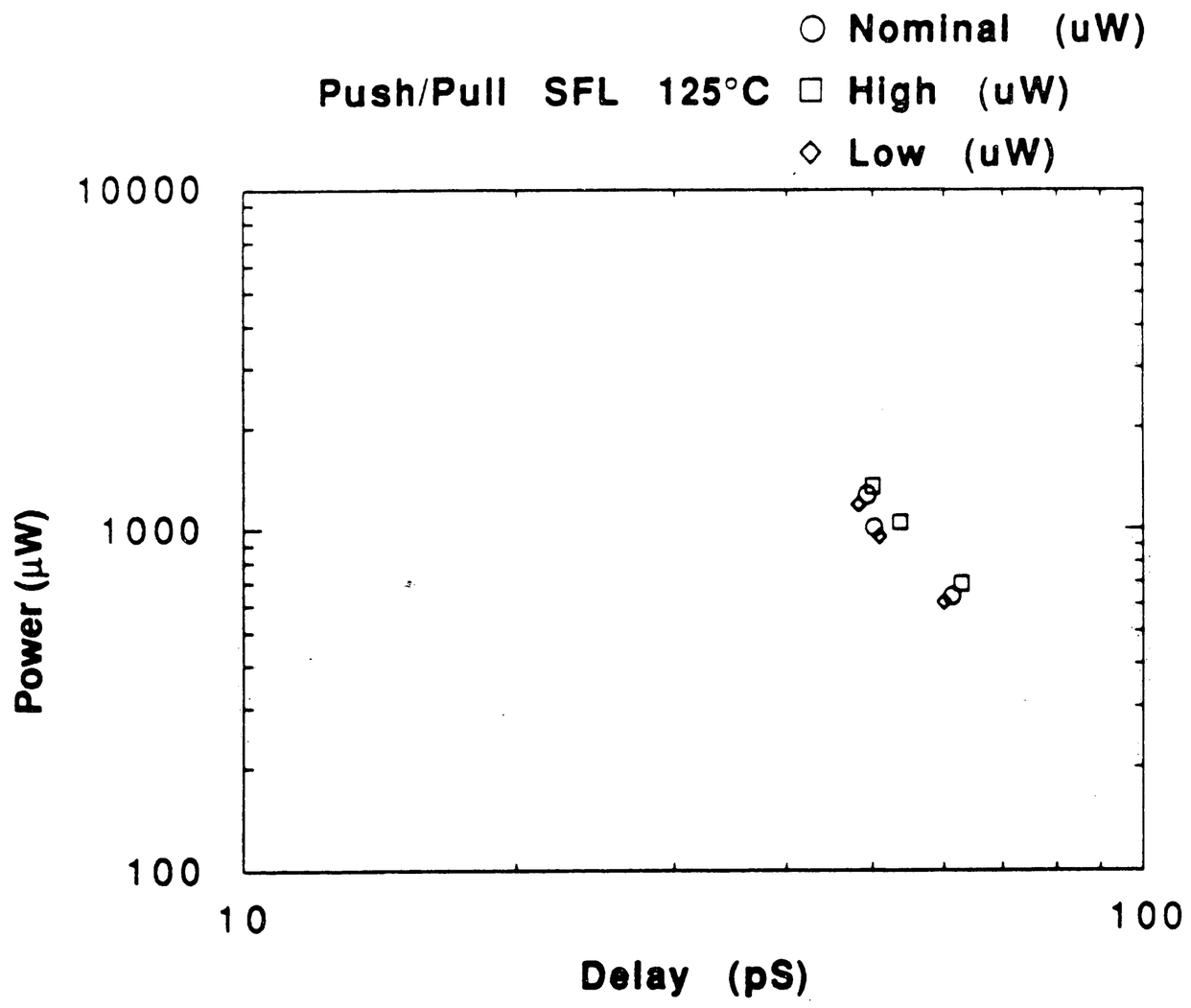


Figure 5.25. Push/Pull SFL power delay product at 125° C.

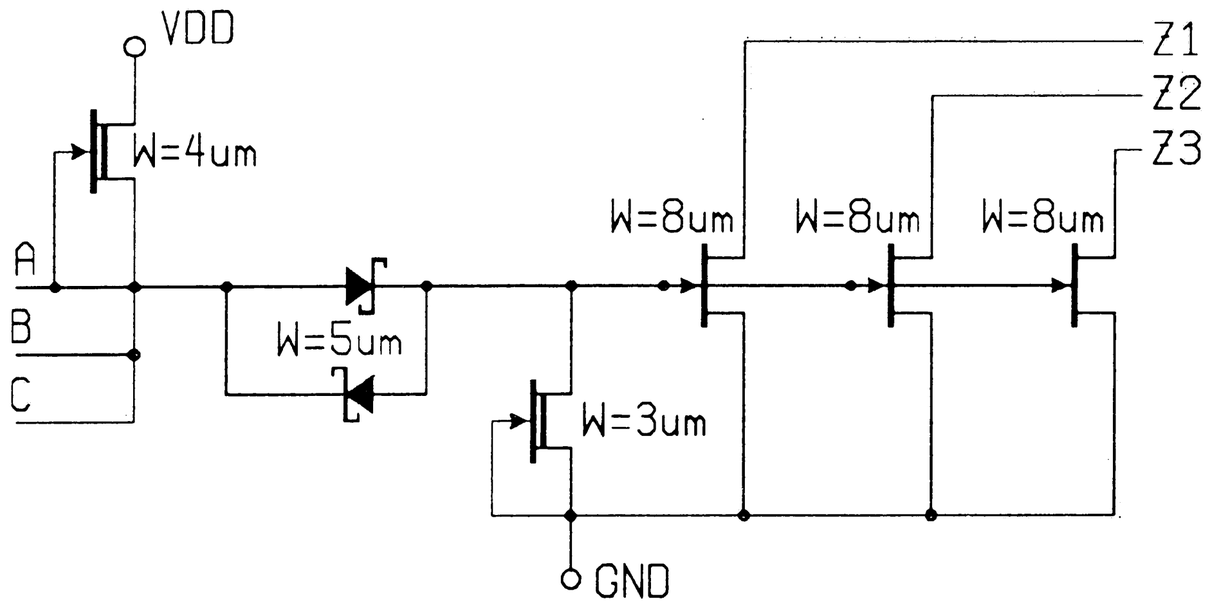


Figure 5.26. FIL 3 input/3 output NAND gate.

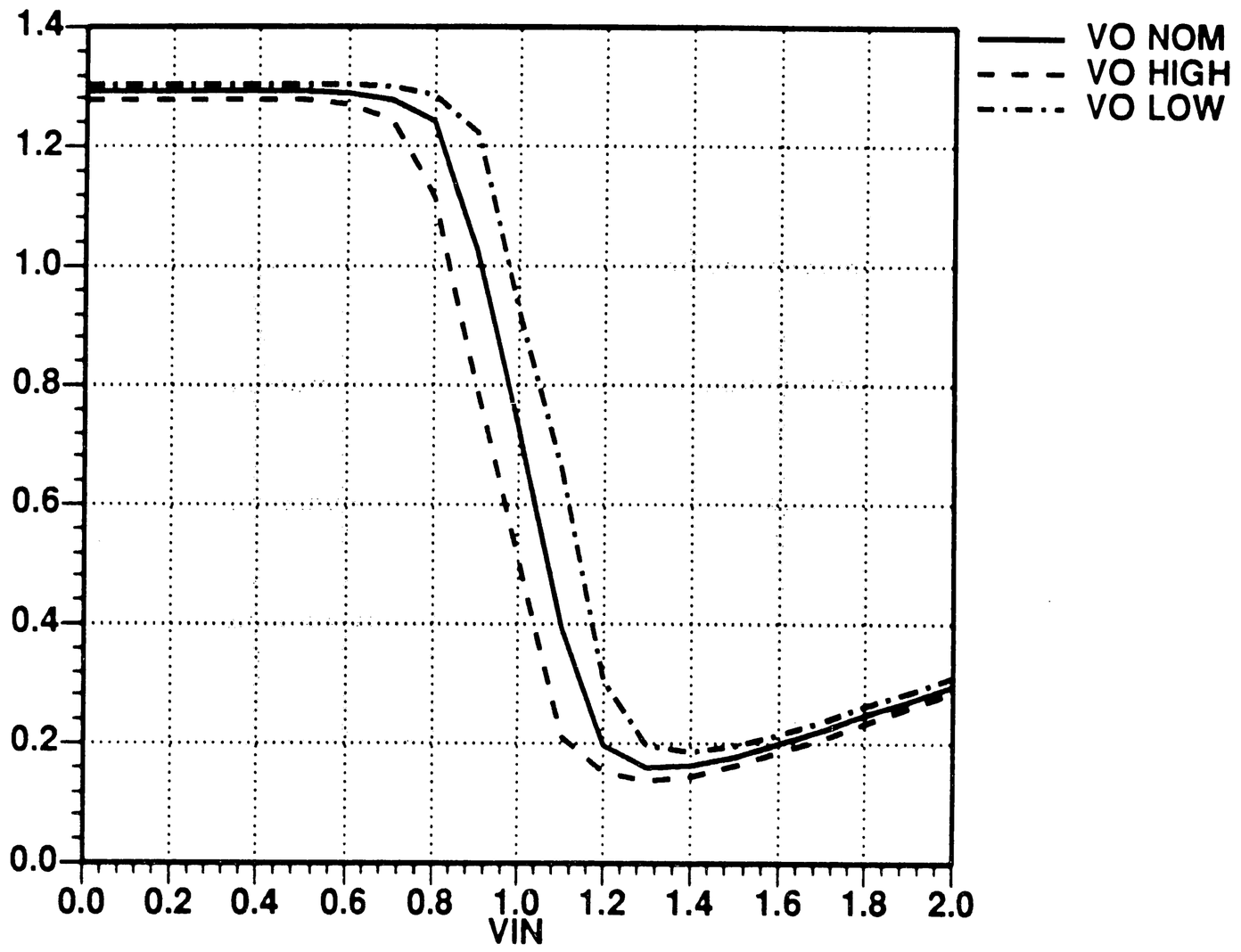


Figure 5.27. FIL transfer characteristics at 25° C.

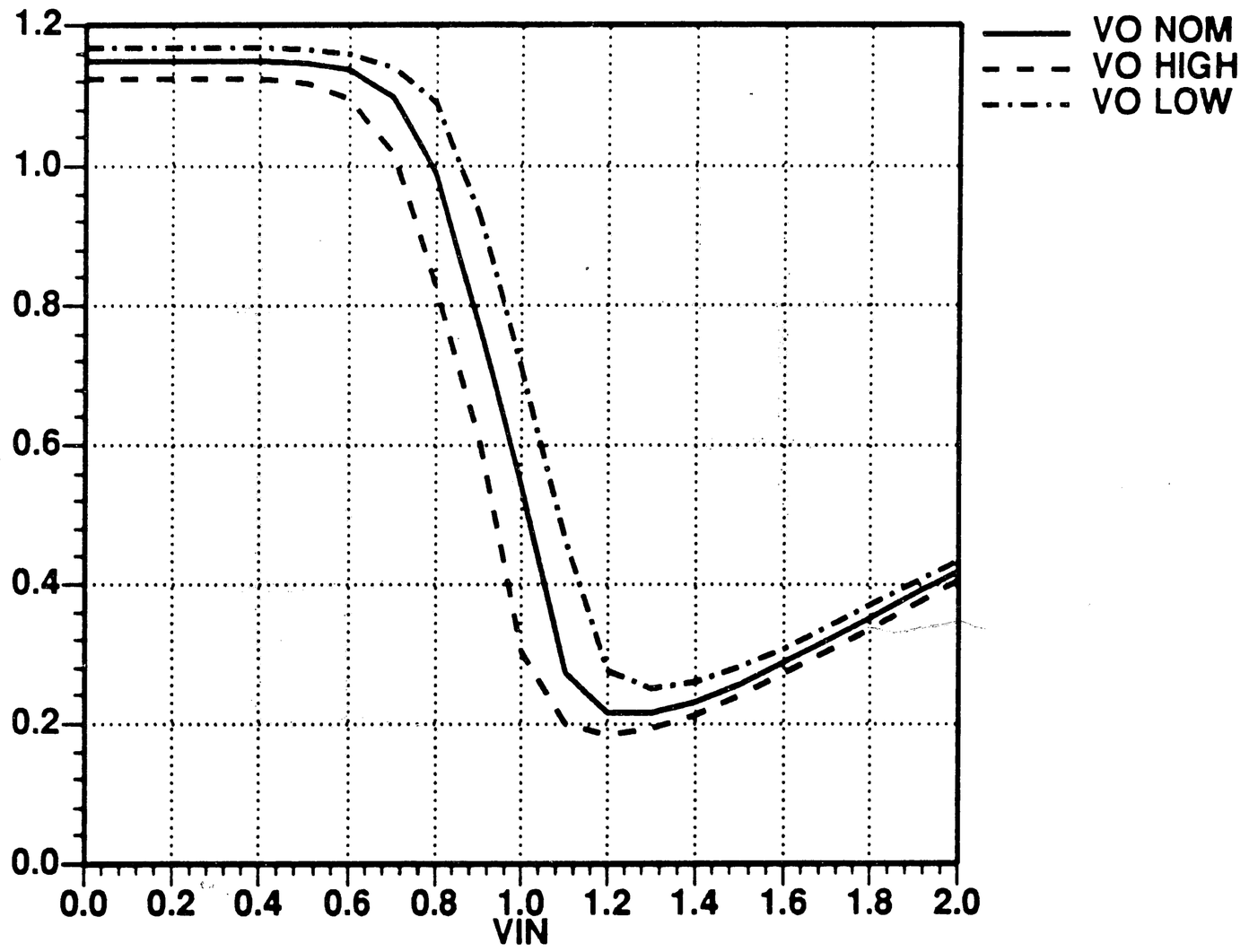


Figure 5.28. FIL transfer characteristics at 125° C.

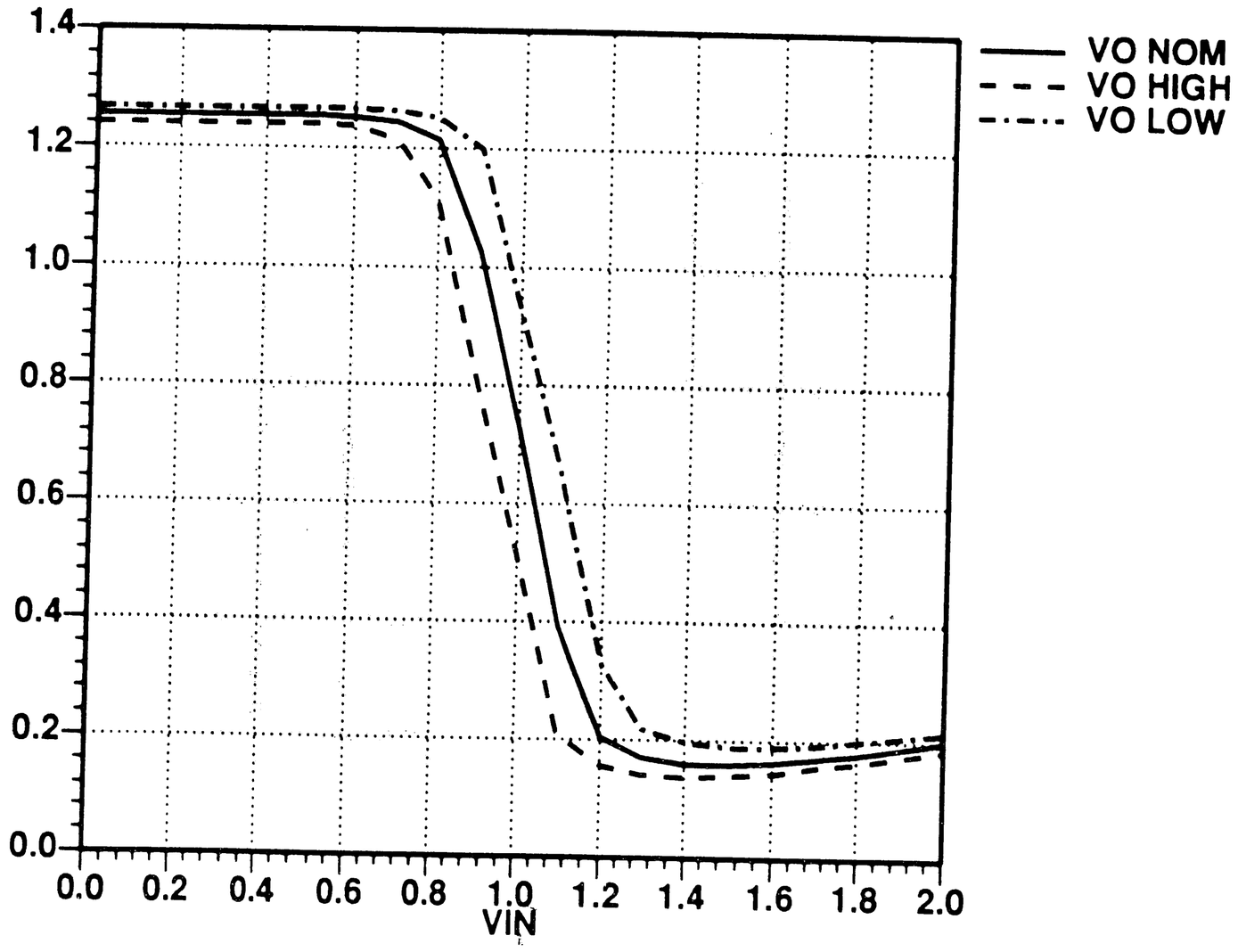


Figure 5.29. FIL transfer characteristics with a FANIN of 3 at 25° C.

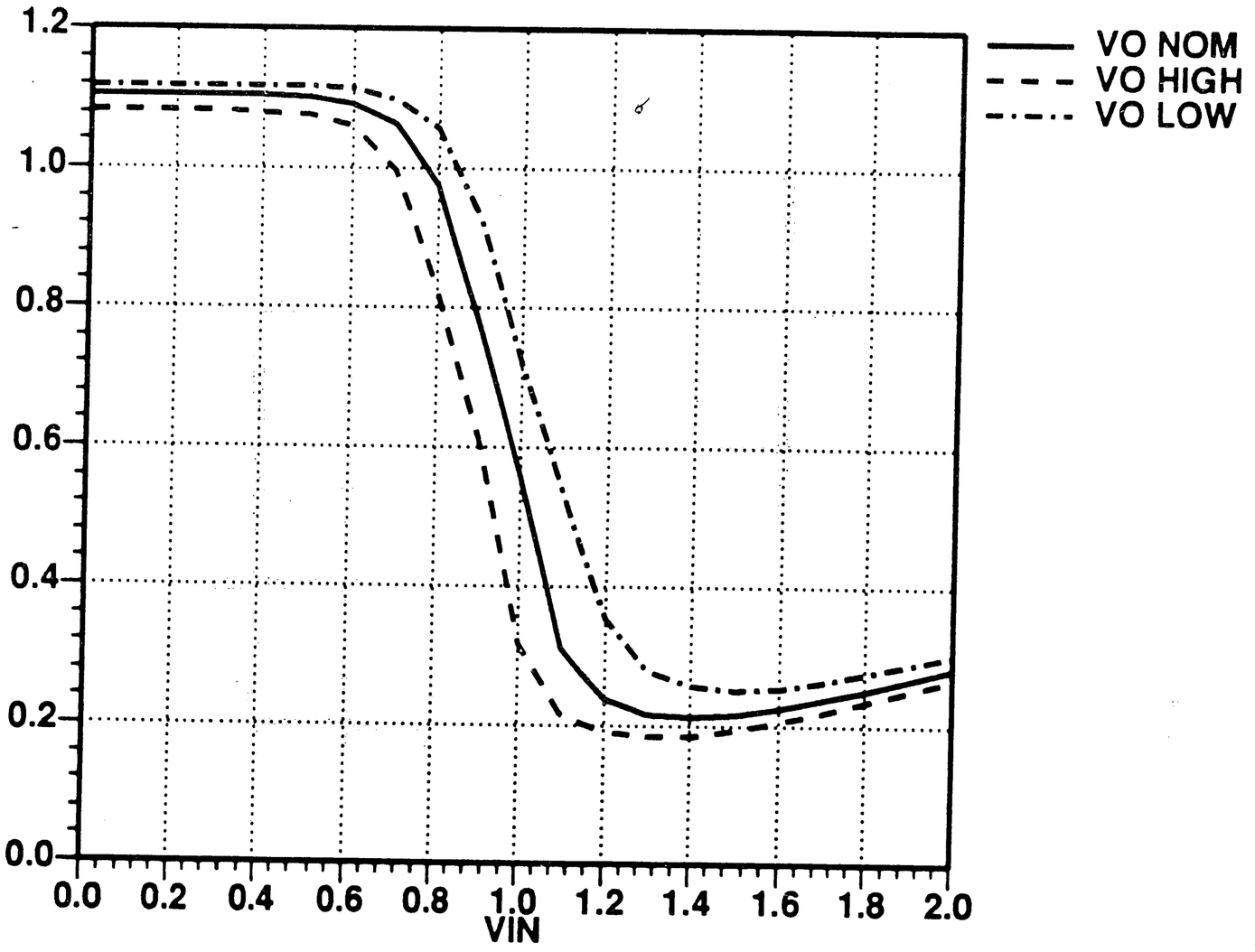


Figure 5.30. FIL transfer characteristics with a FANIN of 3 at 125° C.

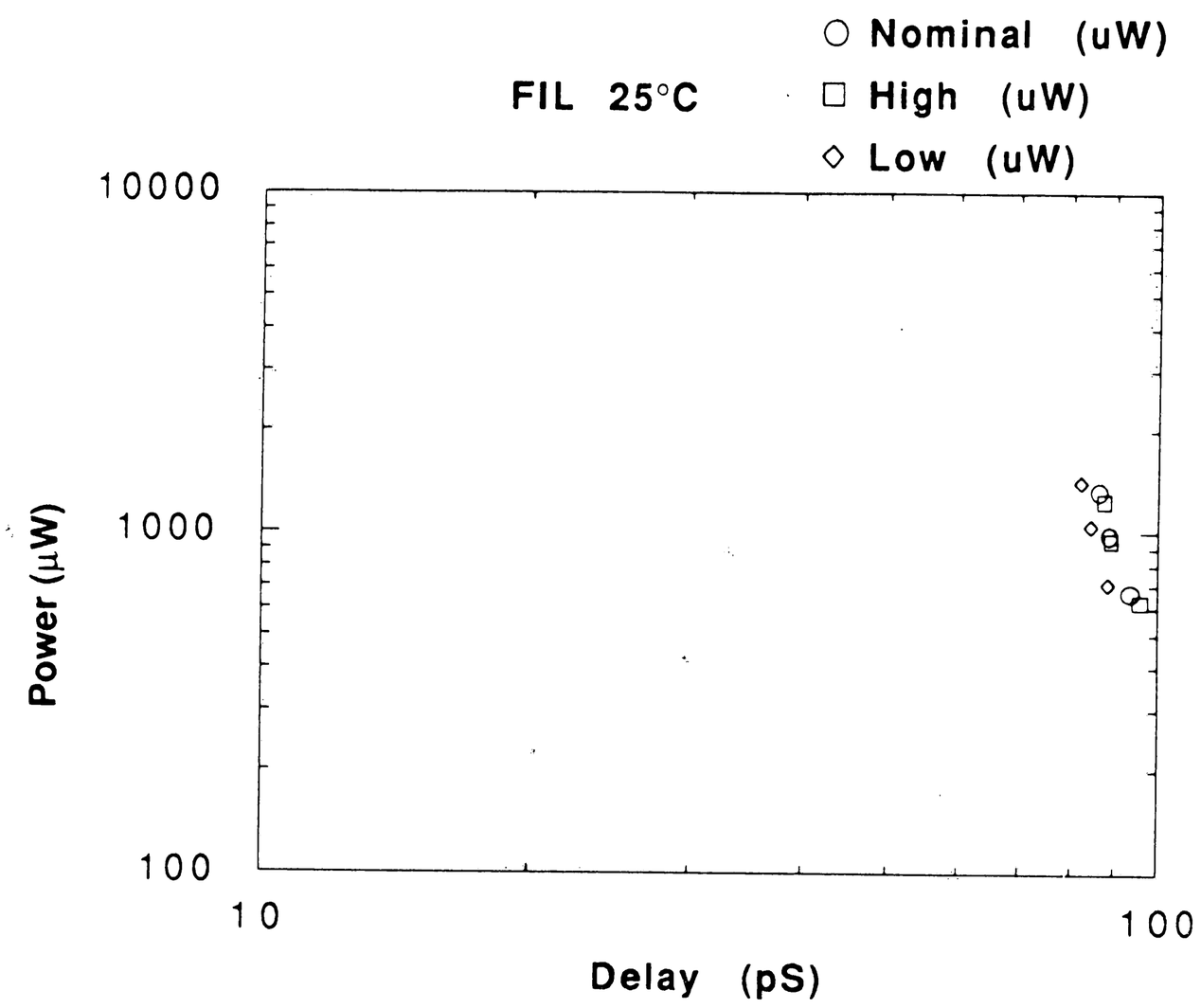


Figure 5.31. FIL power delay product at 25° C.

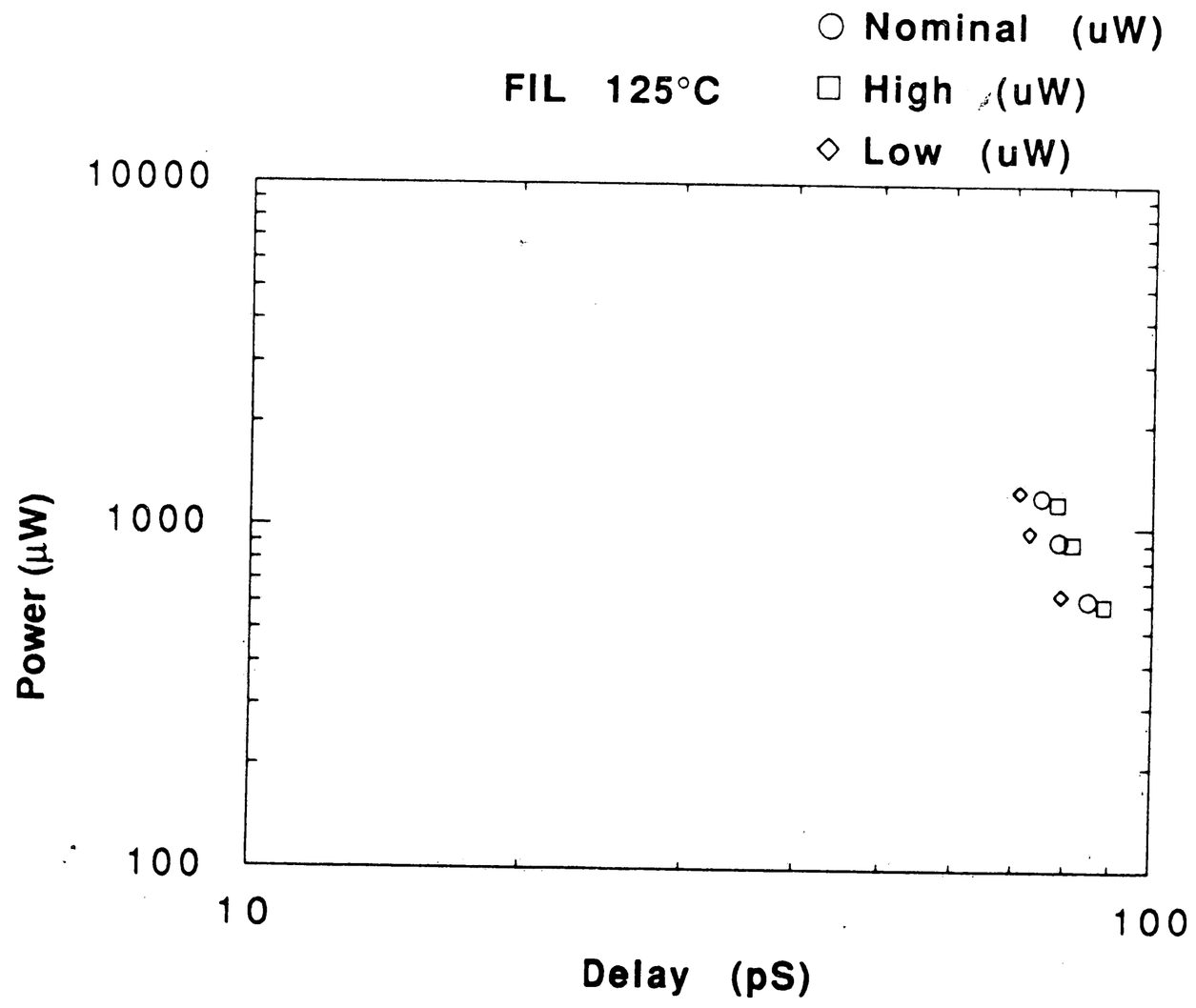


Figure 5.32. FIL power delay product at 125° C.

CHAPTER 6

CONCLUSION

Four logic families suitable for LSI GaAs digital integrated circuit technology have been analyzed and simulated. The logic families are DCFL, SFL, Push/pull SFL, and FIL. The analysis shows that DCFL has low propagation delay and low power dissipation and can achieve high circuit density. However, the family has very low noise margins and large circuits will have poor yields given the present technology and process variations. The SFL logic family is a major improvement over DCFL and the logic families mentioned in the beginning of Chapter 4. This family is robust enough to implement LSI circuits using present GaAs HFET technology. The major drawback of SFL compared to DCFL is the high power dissipation, longer propagation delay, and complicated structure. The analysis of push/pull SFL shows that this family is a high-speed, low power logic families, and has good noise margins. This family rivals DCFL in power delay product comparison, yet has higher noise margins. FIL is a current steering logic family similar to Integrated Injection Logic. The FIL logic family has high noise margins and low power dissipation. However, FIL is very sensitive to fanout loading due -to the Miller capacitance effect. Miller capacitance effect also makes DCFL sensitive, however, FIL is much more sensitive due to the multiple open drain outputs.

One of the most important characteristics of a logic family in LSI and VLSI is the ability to implement complex gates with a single gate delay. It has been shown that this is not possible with DCFL due to the small noise margins. The other logic families can implement multiplexers, OR/AND/INVERT (AND/OR/INVERT) gates, and clocked latches using complex gates. This capability makes the SFL and FIL logic families more competitive than DCFL in increasing circuit performance, density, and reducing chip power dissipation.

The simulations also show that the SFL and FIL logic families are better suited for high speed and high density digital ICs' than SDFL. These logic families all operate from a single power supply voltage rather than two. This attribute will result in smaller power supply bus routing and helps reduce chip area. Also, unlike SDFL which is sensitive to DC and AC loading, SFL and FIL logic families can tolerate more device mis-ratioing.

From an analysis of the SFL and FIL power-delay product plots, it can be deduced that these families can deliver the performance of BFL and SCL at lower power dissipation and higher circuit density.

It is apparent from the DC transfer characteristics that poor voltage gain greatly reduces the noise margin of DCFL and SFL circuits. This situation can be helped by increasing the HFET output resistance and transconductance. The

greatest benefit to the DCFL logic family is the increase of the Schottky barrier height which increases the logic families noise margins.

The FIL logic family suffers from the Miller capacitance effect. This problem can be alleviated by increasing the current drive of EFETs. This will result in reducing the pull-down FET width and thus reduce the Miller capacitance. This will make FIL a viable logic family for implementing high performance, low switching noise circuits.

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VITA

Aziz I. Faris earned the degree of Bachelor of Science in Electrical Engineering with Distinction from the Pennsylvania State University in June, 1982. He joined the engineering staff of Western Electric in Reading, PA, and worked on developing automatic test equipment for photonic devices. In 1983, he was a resident visitor at AT&T Bell Labs in Reading, PA working on the development and design of display head electronics for AC plasma displays. In 1986, he joined Bell Labs as a Member of the Technical Staff working on the development of Digital Gallium Arsenide Integrated Circuits for the AT&T/DARPA Pilot Line III. He has developed both standard cell and macrocell libraries for LSI/VLSI digital GaAs integrated circuits.

He is presently working on the development and design of a 32-bit video serializer chip incorporating analog and digital circuits in GaAs and capable of operating up to 2 GHz.